

Hardware User's Manual

CEI-x30 Product Line

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The CEI-x30 ARINC Product Line

Overview

The CEI-x30 ARINC Product Line is a multiple-channel ARINC interface design available in several form factors and channel configurations supporting ARINC 429, ARINC 573/717, Avionics Discrete I/O, and IRIG time synchronization.

Products included in the CEI-x30 ARINC Product Line are listed with their channel configurations and available/optional features in the following table:

Table 1. CEI-x30 ARINC Products

Product Name	Form Factor	ARINC 429 Maximum Channel Count	Available/Optional Features
RCEI-530	PCI	16 Receivers 16 Transmitters	ARINC 573/717 Rx/Tx IRIG Timecode Rx/Tx 16 Discrete Inputs 16 Discrete Outputs
RAR-CPCI	Compact PCI	16 Receivers 16 Transmitters	ARINC 573/717 Rx/Tx IRIG Timecode Rx/Tx 16 Bidirectional Discrete Input/Output
RAR-PCIE	PCI Express	16 Receivers 16 Transmitters	ARINC 573/717 Rx/Tx IRIG Timecode Rx/Tx 16 Discrete Inputs 16 Discrete Outputs
RAR-MPCIE	Mini PCI Express	8 Receivers 4 Transmitters	ARINC 573/717 Rx/Tx IRIG Timecode Rx/Tx 4 Bidirectional Discrete Input/Output
RAR-XMC	XMC	16 Fixed Receivers plus 16 Channels either Fixed Transmit or Receive, or Programmable Transmit/Receive	ARINC 573/717 Rx/Tx IRIG Timecode Rx/Tx 4 Discrete Inputs 4 Discrete Outputs

Product Name	Form Factor	ARINC 429 Maximum Channel Count	Available/Optional Features
RAR-XMC-TB	Thunderbolt 3	16 Fixed Receivers plus 16 Channels either Fixed Transmit or Receive, or Programmable Transmit/Receive	ARINC 573/717 Rx/Tx IRIG Timecode Rx/Tx 4 Discrete Inputs 4 Discrete Outputs
RAR-EC	ExpressCard	7 Receivers 4 Transmitters	ARINC 573/717 Rx/Tx IRIG Timecode Rx/Tx 4 Bidirectional Discrete Input/Output
RCEI-830A	PMC	16 Receivers 16 Transmitters	ARINC 573/717 Rx/Tx IRIG Timecode Rx/Tx 4 Discrete Inputs 4 Discrete Outputs
RCEI-830A-TB	Thunderbolt 3	16 Receivers 16 Transmitters	ARINC 573/717 Rx/Tx IRIG Timecode Rx/Tx 4 Discrete Inputs 4 Discrete Outputs
RCEI-830X820	PMC	8 Receivers 8 Transmitters	None
CEI-430	PC/104-Plus	12 Receivers 12 Transmitters	ARINC 573/717 Rx/Tx IRIG Timecode Rx/Tx 16 Bidirectional Discrete Input/Output
RCEI-430A	PC/104-Plus	24 Receivers 4 Transmitters	ARINC 573/717 Rx/Tx IRIG Timecode Rx/Tx 16 Bidirectional Discrete Input/Output
AMC-A30	AMC	12 Receivers 12 Transmitters	IRIG Timecode Rx/Tx 4 Bidirectional Discrete Input/Output

For the RCEI-830A and RCEI-830X820 PMC products, a variety of bus adapter configurations are also available, supporting both front and rear-I/O access for PCI, PCI Express, and CompactPCI platforms. For the RAR-XMC and RAR-MPCIE products, PCI Express bus adapters are available.

Common Features

The CEI-x30 ARINC Product Line incorporates a common firmware design across all products. Features available on most CEI-x30 products include the following, with IRIG optional on many products.

General Features

- 64-bit 1 microsecond resolution on-board timer
- Fixed ARINC 429 Receive Threshold Levels

- IRIG-B reception supporting AM or DC/TTL input
- IRIG-B generator supporting DC/TTL output

ARINC 429 Transmit Features

- Fixed transmit signal levels
- Individually programmable channel configuration attributes:
 - transmit bit rate
 - slew rate
 - automatic parity generation
 - message bit count and gap error injection
- Individual 2048 message aperiodic transmit buffer for each channel
- 2048 entry message scheduler table supporting high accuracy periodic message transmission for all channels (exception of a 1024 entry limit on the CEI-830)
- 1 millisecond periodic message scheduler transmission accuracy

ARINC 429 Receive Features

- Fixed receive threshold levels
- Message label filtering/triggering and PCI event/interrupt generation
- 64-bit message time-stamp with a 1 microsecond resolution
- Individually programmable channel configuration attributes:
 - receive bit rate
 - parity detection
 - message length/gap error detection
- Multiple message buffering schemes:
 - Individual 2048 message circular buffer for each channel
 - 16384 message merged mode receive buffer with individual receive channel merged buffer selection
 - Independent label/SDI field value-based snapshot storage

Device Initialization

The CEI-x30 product line consists of products incorporating either flash-based firmware programmed on the card or firmware downloaded from the host over the PCI Interface via the CEI-x30 API. The firmware load

method is specific to both the bus interface type (PCI versus PCI Express), and each board's bus interface architecture, as described in Table 2.

Table 2. CEI-x30 Product Firmware Load Method

Product Name	Bus Interface	Load Data Width
RCEI-830A RCEI-830X820	PLX PCI9056	8-bit
RCEI-530 RAR-CPCI AMC-A30	PLX PCI9056	32-bit
RAR-EC	PLX PCI9030	32-bit
CEI-430 RCEI-430A	PLX PCI9030	8-bit
RAR-XMC RAR-PCIE RAR-MPCIE	FPGA PCI Express Core	N/A

PCI Express Device Configuration

For all PCI Express based devices, (RAR-PCIE, RAR-MPCIE, and RAR-XMC), the ARINC firmware load is programmed in an onboard Flash memory device at the factory and automatically loaded into the FPGA at power-up. Once the FPGA has been successfully configured, the BAR0 memory region reflects the Host Memory Map interface described in the chapter “CEI-x30 Hardware Interface”, section called “Host Memory Map”.

Infield firmware updates are available via board-specific Flash Programmer Utility located in the CEI-x30-SW software distribution when installed for an applicable board. This Windows-only executable is available in the CEI-x30-SW Shortcuts→Tools and Utilities folder shortcut.

Configuring a PCI Bus Device FPGA

For all PCI bus based devices, the firmware load is downloaded from the CEI-x30 API through the PCI bus Interface as part of the board initialization process. The firmware is compiled into the API source, so the firmware version incorporated into these boards is based on the CEI-x30-SW distribution used.

PCI bus based CEI-x30 device FPGA's are configured using the following procedure:

1. Set the software reset bit in the PLX CNTRL register.
2. Delay for at least one millisecond.

3. Clear the software reset bit in the PLX CNTRL register.
4. Delay for at least 100 milliseconds to allow FPGA configuration memory to clear.
5. Restore the local configuration registers by reloading from the serial EEPROM (cleared by the software reset). Do this by setting and then clearing the reset bit of the PLX CNTRL register.
6. Set the local address space 0 bus region descriptor in the respective PLX register (and GPIO registers for the PCI9030) to configure the FPGA into the programming mode.
7. Download the FPGA contents using the appropriate data width, by writing to any location in the BAR2 memory region (word offset 0x0005 is recommended)
8. Reset the local address space 0 bus region descriptor in the respective PLX register (and GPIO registers for the PCI9030) to clear the FPGA programming mode.
9. After a brief delay, verify that the FPGA DONE pin is high. A high level indicates that the FPGA was successfully configured.

Once the FPGA has been successfully configured, the BAR2 memory region reflects the Host Memory Map interface described in the chapter “CEI-x30 Hardware Interface”, section called “Host Memory Map”.

Multiprotocol Boards

The CEI-x30 ARINC common firmware design is also included in the **RAR15XF** and **RAR15-XMC-IT** multiprotocol product configurations, supporting both MIL-STD-1553 and ARINC 429. While not considered a standard product within the CEI-x30 ARINC product line, the respective software distribution CEI-x30-SW supports any of the Abaco Systems multiprotocol boards in which the CEI-x30 common ARINC firmware design has been implemented.

Summary

Each of the products in the CEI-x30 ARINC Product Line is described in detail in chapters 2 through 14, with specific information regarding the respective form factor and I/O connector pin-out. For more specific information regarding CEI-x30 features and firmware, see the chapter titled “CEI-x30 Product Features”. For information regarding the CEI-x30-SW distribution and application programmer’s interface, see the CEI-x30-SW Software User Manual.

CEI-830 / RCEI-830A

Overview

The RCEI-830A is a form/function compatible design update to the original, discontinued CEI-830 product, and unless a deviation is explicitly stated, any RCEI-830A reference in this document applies to the CEI-830.

The RCEI-830A card is a multiple-channel ARINC interface available in several configurations. When configured as the RCEI-830A-1616, this product includes thirty-two ARINC 429 channels, (sixteen receivers and sixteen transmitters), in a PMC form-factor. Configurations are available supporting various ARINC 429 channel counts, ARINC 573/717, Avionics Discrete I/O, and IRIG time synchronization. A variety of bus adapter configurations are also available, supporting Thunderbolt 3, PCI Express, PCI and CompactPCI platforms. For additional information related to operating the RCEI-830A in a Thunderbolt 3 environment refer to the “TB3-TO-CMC-LP Thunderbolt™ 3 Expansion Adapter User's Guide” that is included with the RCEI-830A-TB product and available in the CEI-x30-SW distribution *Documentation* folder. The latest version is available at https://www.abaco.com/TB3LP_guide.

RCEI-830A Specifications

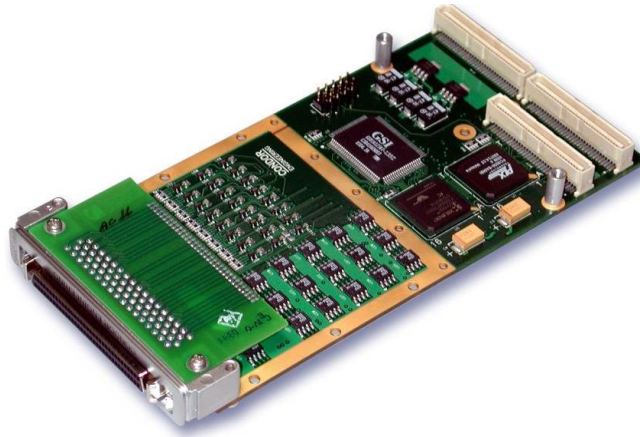


Figure 1. CEI-830

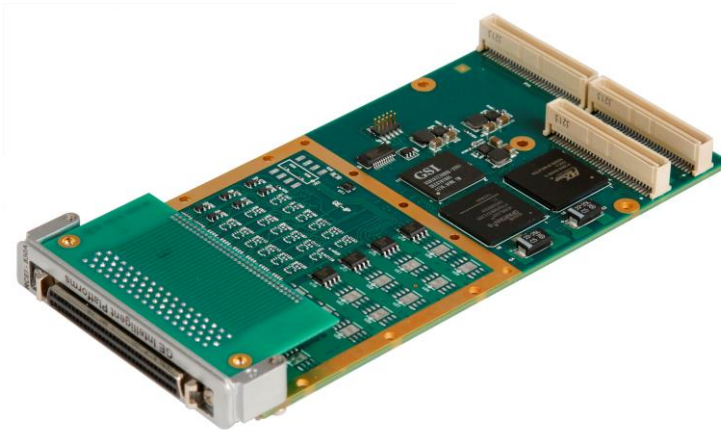


Figure 2. RCEI-830A

The RCEI-830A is a multiple channel, multiple protocol interface built to the PMC standard IEEE-P1386.1.

PMC/PCI Interface

- Standard single-width CMC module per IEEE-P1386.1 draft standard
- +5V and +3.3V PCI signaling compatibility and universal keying
- 66 MHz, 32-bit PCI operation

Transmit Channels

- Up to sixteen independent differential serial transmit channels
- Automatic parity generation
- 2048 message transmit buffer for each channel
- Baud rate/slew rate software-programmable for each channel
- 2048 (RCEI-830A) or 1024 (CEI-830) entry message table supporting scheduled message transmission for all channels

Receiver Channels

- Up to sixteen independent, differential receive channels
- 2048 message buffered mode receive buffer for each channel.
- 16384 message merged mode receive buffer
- Label/SDI message independent snapshot storage for each channel
- Independent merged/individual receive buffer operation.
- 64-bit, 1 μ sec resolution message time-tag
- Parity error detection

Avionics Discrete Input and Output

- Four dedicated avionics-level discrete channels
- Output may switch to ground up to 500mA
- Fixed input threshold of 2.7 +/- 0.2 volts [CEI-830]
- Fixed input threshold of 2.0 +/- 0.3 volts [RCEI-830A]

IRIG Input and Output

- IRIG-B Time-code receiver and transmitter

Typical Power Consumption

Table 3. CEI-830 Power Consumption

+3.3V	+5V	+12V	-12V
500 mA	50 mA	100 mA (no TX Loads)	100 mA (no TX Loads)

Table 4. RCEI-830A Power Consumption

+3.3V	+5V	+12V	-12V
0 mA	125 mA	100 mA (no TX Loads)	100 mA (no TX Loads)

Operating Temperature

-40 to +85 °C

Weight

3.6 ounces

PCI Memory Map

The following table summarizes the PCI memory map interface definition for the RCEI-830A.

Table 5. RCEI-830A PCI Memory Map

Region	Type	Size	Description
configuration	configuration	64 bytes	PCI configuration space
PCI BAR0	memory	512 bytes	PCI9056 memory-mapped local configuration registers
PCI BAR1	I/O	256 bytes	PCI9056 I/O-mapped local configuration registers, unused
PCI BAR2	memory	512K bytes	RCEI-830A host interface
PCI BAR3	n/a	0	not used
PCI BAR4	n/a	0	not used
PCI BAR5	n/a	0	not used

I/O Connections

Input /Output Connectors

At publication of this document, the following mating connector was compatible with the 68-pin SCSI connector used on the RCEI-830A. The Abaco Systems adapter cable CONSCSI3-6 is available for this connection.

Table 6. RCEI-830A Input/Output Connectors

Part No.	Description	Manufacturer
1-5750913-7	Front Panel 68 pin SCSI-3	AMP/Tyco

Input/Output Connector Pin-out

The different RCEI-830A product configurations have specific channel pin-out definitions based on the number of channels and protocols installed. Table 7 describes both the optional 68-pin front panel and P14 mezzanine I/O connector pin-out for the ARINC 429 version of the RCEI-830A module. The exact ARINC 429 channel pin-out depends on the number of receivers and transmitters configured on your RCEI-830A. Table 8 describes the pin-out differences for the -J version of the RCEI-830A; these pins support ARINC 573/717 protocols on the pins used by the upper channels on non-J configurations. Table 9 describes the pin-out differences for the N configuration, supporting Discrete I/O on the pins assigned to the upper channels of the non-N configurations.

Additionally, the P14 mezzanine I/O connector routes the first fifteen ARINC 429 transmit and receive channels, the J configuration ARINC 573/717 channels, and up to two optional Discrete I/O channels.

To externally wrap ARINC signals, connect the transmitter signals to the respective receiver signals, TXnA to RXnA and TXnB to RXnB.

Figure 3 shows the view facing the receptacles of a 68-pin Front-Panel P1 Receptacle Connector (SCSI-3-compatible with Rails and Latch Blocks).

Table 7. RCEI-830A I/O Connections

Signal	Front Panel (P1)	P14 I/O Connector	Signal	Front Panel (P1)	P14 I/O Connector
RX1A	1	63	RX1B	35	64
RX2A	2	61	RX2B	36	62
RX3A	3	59	RX3B	37	60
RX4A	4	57	RX4B	38	58
RX5A	5	55	RX5B	39	56
RX6A	6	53	RX6B	40	54
RX7A	7	51	RX7B	41	52
RX8A	8	49	RX8B	42	50
RX9A	9	47	RX9B	43	48
RX10A	10	45	RX10B	44	46
RX11A	11	43	RX11B	45	44
RX12A	12	41	RX12B	46	42
RX13A	13	39	RX13B	47	40
RX14A	14	37	RX14B	48	38
RX15A	15	35	RX15B	49	36
RX16A	16	N/A	RX16B	50	N/A
TX1A	17	33	TX1B	51	34
TX2A	18	31	TX2B	52	32
TX3A	19	29	TX3B	53	30
TX4A	20	27	TX4B	54	28
TX5A	21	25	TX5B	55	26
TX6A	22	23	TX6B	56	24
TX7A	23	21	TX7B	57	22
TX8A	24	19	TX8B	58	20
TX9A	25	17	TX9B	59	18
TX10A	26	15	TX10B	60	16
TX11A	27	13	TX11B	61	14
TX12A	28	11	TX12B	62	12
TX13A	29	9	TX13B	63	10
TX14A	30	7	TX14B	64	8
TX15A	31	5	TX15B	65	6
TX16A	32	N/A	TX16B	66	N/A
IRIGRX+	33	3	IRIGRX-	67	4
IRIGTX	34	1	Gnd (note)	68	2

Note:

The ground pins are provided as Discrete I/O return lines or for shielding, as necessary.

Table 8. RCEI-830A-xxxx-J I/O Connection for ARINC 573/717

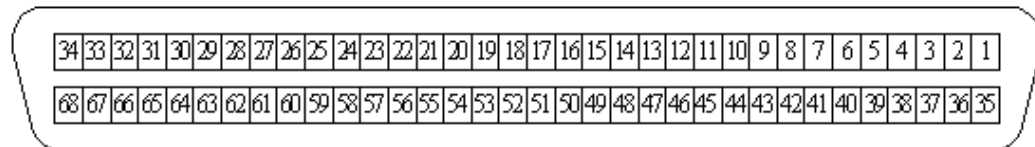
Signal	Front Panel (P1)	P14 I/O Connector	Signal	Front Panel (P1)	P14 I/O Connector
ARINC 717 BPRZ RXA	14	37	ARINC 717 BPRZ RXB	48	38
ARINC 717 HBP RXA	15	35	ARINC 717 HBP RXB	49	36
Reserved	16	N/A	Reserved	50	N/A
...
ARINC 717 TXA (note)	30	7	ARINC 717 BPRZ TXB	64	8
ARINC 717 HBP TXB	31	5	Reserved	65	6
Reserved	32	N/A	Reserved	66	N/A

Note:

The ARINC 573/717 TXA (High) signal is supported on this pin for both the BPRZ and HBP protocols. The selected protocol processed is based on the selection of the ARINC 717 HBP and BPRZ Encoding bits in the respective Transmit Channel Configuration register. See the API routine AR_SET_573_CONFIG for the method to define the ARINC 573/717 active encoding selection for this output pin.

Table 9. RCEI-830A-xxxxN I/O Connection for Discrete I/O

Signal	Front Panel (P1)	P14 I/O Connector	Signal	Front Panel (P1)	P14 I/O Connector
Discrete Input 1	15	35	Discrete Input 2	49	36
Discrete Input 3	16	N/A	Discrete Input 4	50	N/A
...
Discrete Output 1	31	5	Discrete Output 2	65	6
Discrete Output 3	32	N/A	Discrete Output 4	66	N/A

**Figure 3. RCEI-830A P1 68-pin Front-Panel Connector**

Optional RCONSCSI-N-D37-1 Adapter Cable

An optional adapter cable is available to provide a connection which is ARINC 429 and Discrete I/O pin-compatible with the RAR-EC/(R)CEI-715 adapter cables (CONRAR-EC, CONCEI-715, RCONCEI-715A), via the RCONSCSI-N-D37-1 (1320-109-8) cable.

RCONSCSI-N-D37-1 Adapter Cable Pin-out

The pin-out for the RCONSCSI-N-D37-1 Adapter Cable 37-pin D-Subminiature receptacle connector is shown below:

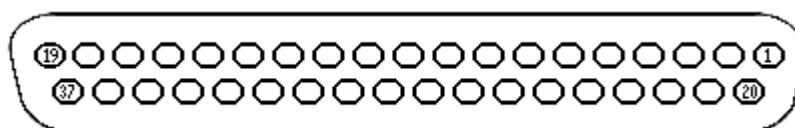


Figure 4. RCONSCSI-N-D37-1 Connector – View Facing Connector

Table 10. RCONSCSI-N-D37-1 Adapter Cable I/O Connections

Adapter Pin	SIGNAL	Adapter Pin	SIGNAL
1	RX1A	20	RX1B
2	RX2A	21	RX2B
3	RX3A	22	RX3B
4	RX4A	23	RX4B
5	RX5A	24	RX5B
6	RX6A	25	RX6B
7	RX7A	26	RX7B
9	RX8A	28	RX8B
10	TX1A	29	TX1B
11	TX2A	30	TX2B
12	TX3A	31	TX3B
13	TX4A	32	TX4B
14	Discrete I/O #1	33	Discrete I/O #2
15	Discrete I/O #3	34	Discrete I/O #4
17	Ground	36	Ground
18	IRIG TX	37	IRIG RX-
19	IRIG RX+		

Notes:

- 1 The ground pins are provided as Discrete I/O return lines or for shielding, as required.

IRIG-B Signal Connections

IRIG-B time (AM or DC/TTL) may be received via signals IRIGRX+ and IRIGRX- (see Table 7). The following IRIG formats are accepted.

Table 11. RCEI-830A IRIG Signal Formats

Format	Modulation Frequency	Frequency/Resolution	Coded Expressions
B	0, 1	0, 2	0, 1, 2, 3

Upon completion of the program load, the RCEI-830A initiates IRIG B002 (DC/TTL) transmission from the onboard IRIG encoder via the IRIGTX signal (see Table 7). The IRIGTX signal can source/sink 16 mA at valid TTL levels.

To externally wrap the IRIG generator to the IRIG receiver, connect the IRIGTX signal to IRIGRX+ input, and connect the IRIGRX- input to Ground.

R830RX

Overview

Note

This product has been discontinued.

The R830RX card is a receive-only version of the CEI-830 ARINC interface in a PMC form-factor, with configurations optionally supporting IRIG time synchronization. A variety of bus adapter configurations are also available, supporting both front and rear-I/O access for PCI, PCI Express, and CompactPCI platforms.

R830RX Specifications



Figure 5. R830RX

The R830RX is a multiple channel ARINC receive-only interface built to the PMC standard IEEE-P1386.1.

PMC/PCI Interface

- Standard single-width CMC module per IEEE-P1386.1 draft standard
- +5V and +3.3V PCI signaling compatibility and universal keying
- 66 MHz, 32-bit PCI operation

Receiver Channels

- Up to thirty-two independent, differential receive channels
- 1024 message buffered mode receive buffer for each channel
- 16384 message merged mode receive buffer
- Label/SDI message independent snapshot storage for each channel
- Independent merged/individual receive buffer operation
- 64-bit, 1 μ sec resolution message time-tag
- Parity error detection

IRIG Input and Output

- IRIG-B Time-code receiver and transmitter

Typical Power Consumption

Table 12. R830RX Power Consumption

+3.3V	5V
250mA	10mA

Operating Temperature

-40 to +85 °C

Weight

3.6 ounces, maximum

PCI Memory Map

The following table summarizes the PCI memory map interface definition for the R830RX.

Table 13. R830RX PCI Memory Map

Region	Type	Size	Description
configuration	configuration	64 bytes	PCI configuration space
PCI BAR0	memory	512 bytes	PCI9056 memory-mapped local configuration registers
PCI BAR1	I/O	256 bytes	PCI9056 I/O-mapped local configuration registers, unused
PCI BAR2	memory	512K bytes	R830RX host interface
PCI BAR3	unused	0	not used
PCI BAR4	unused	0	not used
PCI BAR5	unused	0	not used

I/O Connections

Mating Connectors

At publication of this document, the following mating connector was compatible with the 68-pin (P1) SCSI connector provided on the R830RX front panel (bezel). The Abaco Systems adapter cable CONSCSI3-6 is available for this connection.

Table 14. R830RX P1 Input/Output Connector

Connector	Part No	Description	Manufacturer
P1	1-5750913-7	Front Panel 68 pin SCSI-3	AMP/Tyco

Input /Output Connector Pin-out

Table 15 describes both the optional 68-pin front panel and P14 mezzanine I/O connector pin-out for the R830RX. The exact ARINC 429 channel pin-out depends on the number of receivers configured on your R830RX. The P14 mezzanine I/O connector routes all thirty-two ARINC 429 receive channels. Figure 6 shows the view facing the receptacles of a 68-pin Front-Panel P1 (bezel) Receptacle Connector (SCSI-3-compatible with Rails and Latch Blocks).

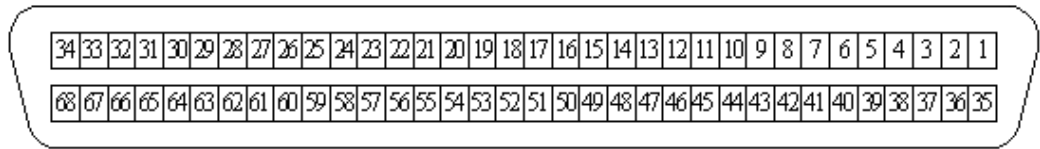


Figure 6. R830RX P1 68-pin Front-Panel Connector

Table 15. R830RX P1 ARINC I/O Connections

Signal	Front Panel (P1)	P14 I/O Connector	Signal	Front Panel (P1)	P14 I/O Connector
RX1A	1	2	RX1B	35	1
RX2A	2	4	RX2B	36	3
RX3A	3	6	RX3B	37	5
RX4A	4	8	RX4B	38	7
RX5A	5	10	RX5B	39	9
RX6A	6	12	RX6B	40	11
RX7A	7	14	RX7B	41	13
RX8A	8	16	RX8B	42	15
RX9A	9	18	RX9B	43	17
RX10A	10	20	RX10B	44	19
RX11A	11	22	RX11B	45	21
RX12A	12	24	RX12B	46	23
RX13A	13	26	RX13B	47	25
RX14A	14	28	RX14B	48	27
RX15A	15	30	RX15B	49	29
RX16A	16	32	RX16B	50	31
RX17A	17	34	RX17B	51	33
RX18A	18	36	RX18B	52	35
RX19A	19	38	RX19B	53	37
RX20A	20	40	RX20B	54	39
RX21A	21	42	RX21B	55	41
RX22A	22	44	RX22B	56	43
RX23A	23	46	RX23B	57	45
RX24A	24	48	RX24B	58	47
RX25A	25	50	RX25B	59	49
RX26A	26	52	RX26B	60	51
RX27A	27	54	RX27B	61	53
RX28A	28	56	RX28B	62	55
RX29A	29	58	RX29B	63	57
RX30A	30	60	RX30B	64	59
RX31A	31	62	RX31B	65	61
RX32A	32	64	RX32B	66	63
TXA ¹			TXB ¹		

Signal	Front Panel (P1)	P14 I/O Connector	Signal	Front Panel (P1)	P14 I/O Connector
IRIGTX+ ² IRIGRX+ ³			IRIGTX- ² IRIGRX- ³		
IRIGRX+	33	N/A	IRIGRX-	67	N/A
Gnd ⁴	34	N/A	Gnd ⁴	68	N/A

Notes:

1. When the jumper pin pairs J4 and J5 are shorted and Bit 4 of the Global Enable Register is set low (0), the on-board transmitter signals TXA and TXB will be enabled and physically shorted to these pins.
2. When the jumper pin pairs for J4 and J5 are shorted and Bit 4 of the Global Enable Register is set high (1), the on-board IRIG Generator signals will be enabled and physically shorted to these pins.
3. Specifically for rear-I/O configurations, when the jumper pin pairs for J2 and J3 are shorted, these I/O pins can then be used for either IRIG time code reception or as the thirty-second ARINC 429 receiver.
4. The ground pins are provided for shielding, as required.

Jumper Connections

The R830RX board contains a set of four special-purpose jumper pin-pairs. Each jumper pin-pair can be shorted using a standard 0.1 inch shunt (not provided); however, the preferred shorting method is wire-wrap or soldered wire. The jumper pin-pairs are located on the component side of the R830RX, labeled J2, J3, J4 and J5.

Jumper pin pairs J2 and J3 are provided specifically for use with IRIG-B signal reception on the R830RX rear-I/O configuration. When the jumper pins across the J2 and J3 pin pairs are shorted, the IRIG Receiver pins IRIGRX+ and IRIGRX- will be physically shorted to P14 pins 63 and 64, respectively. These pins can then be used for either IRIG time code reception or as the thirty-second ARINC 429 receiver, depending on the signal source on the external connection.

Jumper pin pairs J4 and J5 are provided specifically for use with the on-board IRIG generator. When the jumper pins across the J4 and J5 pin pairs are shorted and Bit 4 of the Global Enable Register is set high (1), the on-board IRIG Generator signals + and – will be enabled and physically shorted to ARINC Receive pins RX32A and RX32B, respectively. In this case, pins RX32A and RX32B will not support ARINC 429 reception and should not be connected to an external ARINC transmitter.

An alternate test-only transmitter connection using jumper pin pairs J4 and J5 is also provided. When jumper pin pairs J4 and J5 are shorted and Bit 4 of the Global Enable Register is set low (0), the on-board transmitter signals TXA and TXB will be enabled and physically shorted to ARINC Receive pins RX32A and RX32B, respectively. The output from this *test-*

only transmitter is not compliant with ARINC 429 transmit specifications and in this case, these I/O pins should not be connected to an off-board ARINC transmitter or receiver.

IRIG-B Signal Connections

IRIG-B time (AM or DC/TTL) may be received via signals IRIGRX+ and IRIGRX-. The following IRIG formats are accepted:

Table 16. R830RX IRIG Signal Formats Supported

Format	Modulation Frequency	Frequency/Resolution	Coded Expressions
B	0, 1	0, 2	0, 1, 2, 3

IRIG-B Generator Signal Connections

Upon completion of the program load, the R830RX initiates IRIG B002 (DC/TTL) transmission from the onboard IRIG encoder. To use the output from the IRIG-B generator, it must first be enabled by shorting the jumper pins for both J4 and J5 and setting Bit 4 of the Global Enable Register high (1), (see the routine AR_SET_DEVICE_CONFIG option ARU_IRIG_OUTPUT_ENABLE). Once enabled, the IRIGTX+/- signals can source/sink 16 mA at valid TTL levels on these pins; however, pins RX32A/RX32B will be unavailable for use as an ARINC 429 receiver.

IRIG-B Receiver Signal Connections

IRIG reception via front-I/O is always available on P1 pins 33 and 67. IRIG reception via rear-I/O is only available on P14 pins 63 and 64 when J2 and J3 jumper pins are shorted; however, pins 63 and 64 will then be unavailable for use as an ARINC 429 receiver.

To externally wrap the IRIG receiver to the IRIG generator you must first enable the IRIG-B generator as discussed above. You would then either connect the IRIGTX+ signal to IRIGRX+ input and the IRIGTX- signal to the IRIGRX- input (using front-I/O connections); or optionally (and for rear-I/O connections), short jumper pins J2 and J3.

RCEI-530

Overview

The RCEI-530 card is a multiple-channel ARINC interface, available in several configurations for the PCI platform. When configured as an RCEI-530-1616, this card includes thirty-two ARINC 429 channels, (sixteen receivers and sixteen transmitters.) There are a variety of configurations available supporting various ARINC 429 channel counts, ARINC 573/717, Avionics Discrete I/O, and IRIG time synchronization.

RCEI-530 Specifications

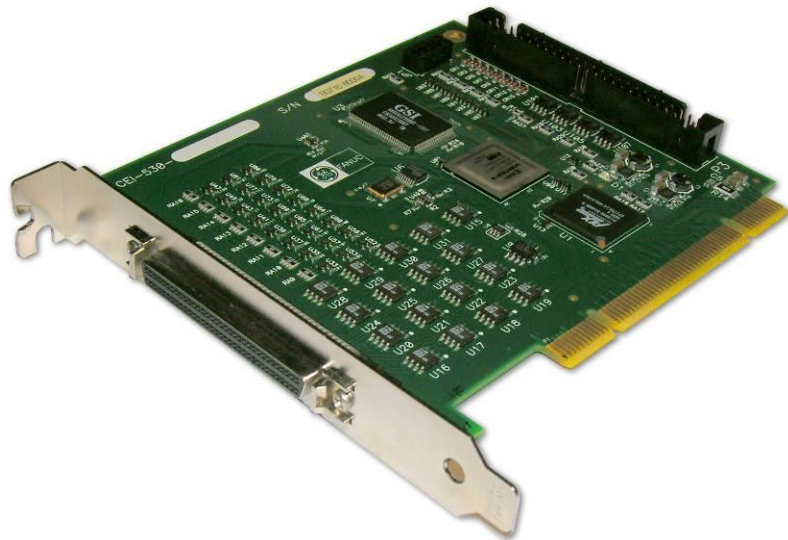


Figure 7. RCEI-530

The RCEI-530 is a multiple channel, multiple protocol interface built to the PCI Local Bus Specification, version 2.2.

PCI Interface

- Standard PCI Interface per the PCI Local Bus Specification Revision 2.2
- +5V and +3.3V PCI signaling compatibility and universal keying
- 66 MHz, 32-bit PCI operation

Transmit Channels

- Up to sixteen independent differential serial transmit channels
- Automatic parity generation
- 2048 message transmit buffer for each channel
- Baud rate/slew rate software-programmable for each channel
- 2048 entry message table supporting scheduled message transmission for all channels

Receiver Channels

- Up to sixteen independent, differential receive channels
- 2048 message buffered mode receive buffer for each channel
- 16384 message merged mode receive buffer
- Label/SDI message independent snapshot storage for each channel
- Independent merged/individual receive buffer operation
- 64-bit, 1 μ sec resolution message time-tag
- Parity error detection

Avionics Discrete Input and Output

- Up to sixteen individual, avionics-level input and output discrete channels
- Output may switch to ground up to 500mA
- Power-up / reset default inactive
- Fixed input threshold of 2.7 +/- 0.2 volts

IRIG Input and Output

- IRIG-B Time-code receiver and transmitter

Typical Power Consumption

Table 17. RCEI-530 Power Consumption

+3.3V	5V	+12V	-12V
500 mA	50 mA	100 mA (no TX Loads) 350mA (sixteen transmitters, max data rate, 400Ω load each)	100 mA (no TX Loads) 350mA (sixteen transmitters, max data rate, 400Ω load each)

Operating Temperature

-40 to +85 °C

Weight

3.6 ounces, maximum

PCI Memory Map

The following table summarizes the PCI memory map interface definition for the RCEI-530.

Table 18. RCEI-530 PCI Memory Map

Region	Type	Size	Description
configuration	configuration	64 bytes	PCI configuration space
PCI BAR0	memory	512 bytes	PCI9056 memory-mapped local configuration registers
PCI BAR1	I/O	256 bytes	PCI9056 I/O-mapped local configuration registers, unused
PCI BAR2	memory	512K bytes	RCEI-530 host interface
PCI BAR3	unused	0	not used
PCI BAR4	unused	0	not used
PCI BAR5	unused	0	not used

I/O Connections

RCEI-530 Outline Drawing

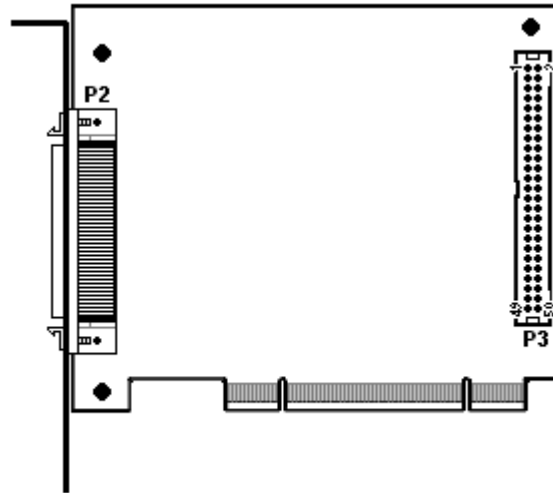


Figure 8. RCEI-530 Outline Drawing

Mating Connectors

At publication of this document, the following mating connector was compatible with the P2 68-pin SCSI connector provided on the RCEI-530 front panel (bezel). The Abaco Systems adapter cable CONSCSI3-6 is available for this connection.

Table 19. RCEI-530 P2 Input/Output Connector

Connector	Part No	Description	Manufacturer
P2	1-5750913-7	Front Panel 68 pin SCSI-3	AMP/Tyco

At publication of this document, the following mating connectors were compatible with the P3 50-pin IDC ribbon connector used for the RCEI-530 Discrete and IRIG I/O, located towards the rear of the RCEI-530 PCB.

Table 20. RCEI-530 P3 Input/Output Connector

Connector	Part No	Description	Manufacturer
P3	1-1658622-0	50 pin Ribbon 0.100 Centers	AMP/Tyco
	3425-6650	50 pin Ribbon 0.100 Centers	3M

ARINC Input /Output Connector Pin-out

Various RCEI-530 product configurations have specific channel pin-out definitions based on the number of channels and protocols included. Table 21 describes the front panel connector pin layout for the RCEI-530. The exact ARINC 429 channel pin-out depends on the number of receivers and transmitters configured on your RCEI-530. For the -J version of the CEI-530, the ARINC 573/717 protocol support pins replace the channel 16 ARINC 429 I/O pins. Note the RCEI-530 I/O pin assignments are pin-compatible with the CEI-520 I/O pin assignments. Figure 9 shows the view facing the receptacles of a 68-pin Front-Panel P2 (bezel) Receptacle Connector (SCSI-3-compatible with Rails and Latch Blocks).

To externally wrap ARINC signals, connect the transmitter signals to the respective receiver signals, TXnA to RXnA and TXnB to RXnB.

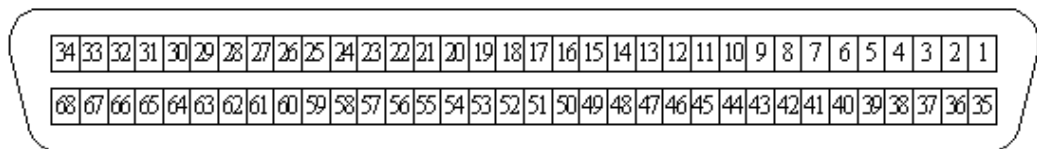


Figure 9. RCEI-530 P2 68-pin Front-Panel Connector

Table 21. RCEI-530 P2 Front Panel ARINC I/O Connections

Signal	P2 Pin	Signal	P2 Pin
TX1A	1	TX1B	35
TX2A	2	TX2B	36
TX3A	3	TX3B	37
TX4A	4	TX4B	38
TX5A	5	TX5B	39
TX6A	6	TX6B	40
TX7A	7	TX7B	41
TX8A	8	TX8B	42
TX9A	9	TX9B	43
TX10A	10	TX10B	44
TX11A	11	TX11B	45
TX12A	12	TX12B	46
TX13A	13	TX13B	47
TX14A	14	TX14B	48
TX15A	15	TX15B	49
TX16A ²	16	TX16B ²	50
Ground ¹	17	Ground ¹	51
RX1A	18	RX1B	52
RX2A	19	RX2B	53
RX3A	20	RX3B	54

Signal	P2 Pin	Signal	P2 Pin
RX4A	21	RX4B	55
RX5A	22	RX5B	56
RX6A	23	RX6B	57
RX7A	24	RX7B	58
RX8A	25	RX8B	59
Ground ¹	26	Ground ¹	60
RX9A	27	RX9B	61
RX10A	28	RX10B	62
RX11A	29	RX11B	63
RX12A	30	RX12B	64
RX13A	31	RX13B	65
RX14A	32	RX14B	66
RX15A	33	RX15B	67
RX16A ²	34	RX16B ²	68

Notes:

- 1 The ground pins are provided for shielding, as required.
- 2 The ARINC 573/717 signals are supported on the respective channel 16 pins for both the BPRZ and HBP protocols. The selected protocol processed is based on the selection of the ARINC 717 HBP and BPRZ Encoding bits in the respective Transmit Channel Configuration register. See the API routine AR_SET_573_CONFIG for the method to define the ARINC 573/717 active encoding selection for this output pin.

Discrete and IRIG Input/Output Connector Pin-out

All RCEI-530 product configurations have the same Discrete and IRIG I/O pin-out definition for the IDC-50 I/O connector located at the rear of the board, pin-compatible with the CEI-520 IDC-50 Discrete I/O pin-out. Figure 10 shows the view facing the receptacles of the P3 IDC-50 I/O Connector.

To externally wrap Discrete I/O channels, connect the output pins to the respective input pins, DOUTn to DINn.

49	47	45	43	41	39	37	35	33	31	29	27	25	23	21	19	17	15	13	11	9	7	5	3	1
50	48	46	44	42	40	38	36	34	32	30	28	26	24	22	20	18	16	14	12	10	8	6	4	2

Figure 10. RCEI-530 P3 50-pin IDC-50 I/O Connector

Table 22. RCEI-530 P3 IDC-50 I/O Connections

Signal	P3 Pin	Signal	P3 Pin
DIN1	1	DOUT8	26
DIN2	2	DOUT9	27
DIN3	3	DOUT10	28
DIN4	4	DOUT11	29
DIN5	5	DOUT12	30
DIN6	6	DOUT13	31
DIN7	7	DOUT14	32
DIN8	8	DOUT15	33
DIN9	9	DOUT16	34
DIN10	10	Ground	35
DIN11	11	Ground	36
DIN12	12	IRIGRX+	37
DIN13	13	IRIGRX-	38
DIN14	14	IRIGTX	39
DIN15	15	Ground	40
DIN16	16	Ground	41
Ground	17	Ground	42
Ground	18	N/C	43
DOUT1	19	N/C	44
DOUT2	20	N/C	45
DOUT3	21	N/C	46
DOUT4	22	N/C	47
DOUT5	23	N/C	48
DOUT6	24	N/C	49
DOUT7	25	Ground	50

Note:

The ground pins are provided as Discrete I/O return lines or for shielding, as required.

IRIG-B Signal Connections

IRIG-B time (AM or DC/TTL) may be received via signals IRIGRX+ and IRIGRX- (see Table 22). The following IRIG formats are accepted:

Table 23. RCEI-530 IRIG Signal Connections

Format	Modulation Frequency	Frequency/Resolution	Coded Expressions
B	0, 1	0, 2	0, 1, 2, 3

Upon completion of the program load, the RCEI-530 initiates IRIG B002 (DC/TTL) transmission from the onboard IRIG encoder via the IRIGTX signal (see Table 22). The IRIGTX signal can source/sink 16 mA at valid TTL levels.

To externally wrap the IRIG generator to the IRIG receiver, connect the IRIGTX signal to IRIGRX+ input, and connect the IRIGRX- input to Ground.

RAR-PCIE

Overview

The RAR-PCIE card is a multiple-channel ARINC interface, available in several configurations for the PCI Express platform. When configured as a RAR-PCIE-1616, this card includes thirty-two ARINC 429 channels, (sixteen receivers and sixteen transmitters.) There are a variety of configurations available supporting various ARINC 429 channel counts, ARINC 573/717, Avionics Discrete I/O, and IRIG time synchronization.

RAR-PCIE Specifications



Figure 11. RAR-PCIE

The RAR-PCIE is a multiple channel, multiple protocol interface built to the PCI Express Base Specification 2.0.

PCI Express Interface

- Standard PCI Express Interface per the PCI Express Card Electromechanical Specification Revision 2.0

Transmit Channels

- Up to sixteen independent differential serial transmit channels
- Automatic parity generation
- 2048 message transmit buffer for each channel
- Baud rate/slew rate software-programmable for each channel
- Each channel includes tri-state capability
- 2048 entry message table supporting scheduled message transmission for all channels

Receiver Channels

- Up to sixteen independent, differential receive channels
- 2048 message buffered mode receive buffer for each channel
- 16384 message merged mode receive buffer
- Label/SDI message independent snapshot storage for each channel
- Independent merged/individual receive buffer operation
- 64-bit, 1 μ sec resolution message time-tag
- Parity error detection

Avionics Discrete Input and Output

- Up to sixteen individual, avionics-level input and output discrete channels
- Output may switch to ground up to 500mA
- Power-up / reset default inactive
- Fixed input threshold of 2.0 +/- 0.2 volts

IRIG Input and Output

- IRIG-B Time-code receiver and transmitter

Typical Power Consumption

Table 24. RAR-PCIE Power Consumption

+3.3V	+12V
600 mA	140 mA (no TX Loads)
	Note: Each additional mA of transmit load current will add an additional mA of +12V supply current.

Operating Temperature

-40 to +75 °C

Weight

3.8 ounces

PCI Memory Map

The following table summarizes the PCI memory map interface definition for the RAR-PCIE.

Table 25. RAR-PCIE PCI Memory Map

Region	Type	Size	Description
configuration	configuration	64 bytes	PCI configuration space
PCI BAR0	memory	512K bytes	RAR-PCIE host interface
PCI BAR1	unused	0	not used
PCI BAR2	unused	0	not used
PCI BAR3	unused	0	not used
PCI BAR4	unused	0	not used
PCI BAR5	unused	0	not used

I/O Connections

RAR-PCIE Outline Drawing

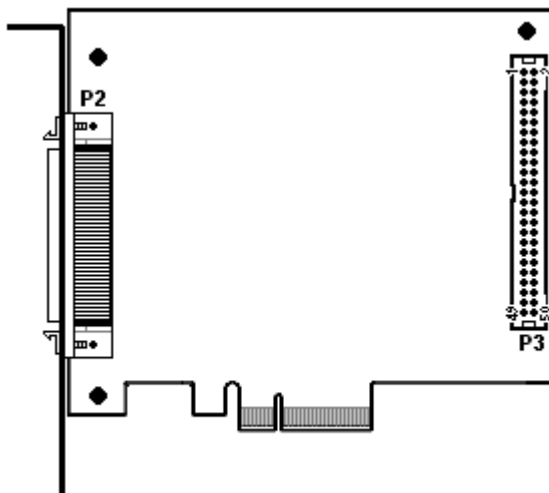


Figure 12. RAR-PCIE Outline Drawing

Mating Connectors

At publication of this document, the following mating connector was compatible with the P2 68-pin SCSI connector provided on the RAR-PCIE front panel (bezel). The Abaco Systems adapter cable CONSCSI3-6 is available for this connection.

Table 26. RAR-PCIE P2 Input/Output Connector

Connector	Part No	Description	Manufacturer
P2	1-5750913-7	Front Panel 68 pin SCSI-3	AMP/Tyco

At publication of this document, the following mating connectors were compatible with the P3 50-pin IDC ribbon connector used for the RAR-PCIE Discrete and IRIG I/O, located towards the rear of the RAR-PCIE PCB.

Table 27. RAR-PCIE P3 Input/Output Connector

Connector	Part No	Description	Manufacturer
P3	1-1658622-0	50 pin Ribbon 0.100 Centers	AMP/Tyco
	3425-6650	50 pin Ribbon 0.100 Centers	3M

ARINC Input/Output Connector Pin-out

Various RAR-PCIE product configurations have specific channel pin-out definitions based on the number of channels and protocols included. Table 28 describes the front panel connector pin-out for the RAR-PCIE. The exact ARINC 429 channel pin-out depends on the number of receivers and transmitters configured on your RAR-PCIE. For the -J version of the RAR-PCIE, the ARINC 573/717 protocol support pins replace the channel 16 ARINC 429 I/O pins. Note the RAR-PCIE I/O pin assignments are pin-compatible with the CEI-520 and RCEI-530 I/O pin assignments. Figure 13 shows the view facing the receptacles of the 68-pin Front-Panel P2 (bezel) Receptacle Connector (SCSI-3-compatible with Rails and Latch Blocks).

To externally wrap ARINC signals, connect the transmitter signals to the respective receiver signals, TXnA to RXnA and TXnB to RXnB.

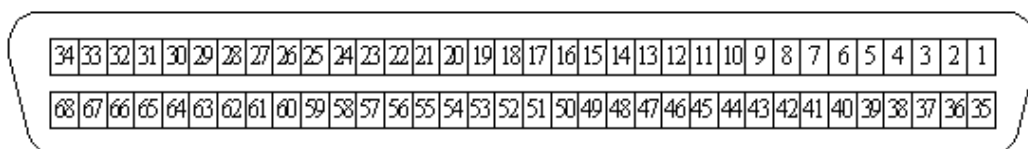


Figure 13. RAR-PCIE P2 68-pin Front-Panel Connector

Table 28. RAR-PCIE P2 Front Panel ARINC I/O Connections

Signal	P2 Pin	Signal	P2 Pin
TX1A	1	TX1B	35
TX2A	2	TX2B	36
TX3A	3	TX3B	37
TX4A	4	TX4B	38
TX5A	5	TX5B	39
TX6A	6	TX6B	40
TX7A	7	TX7B	41
TX8A	8	TX8B	42
TX9A	9	TX9B	43
TX10A	10	TX10B	44
TX11A	11	TX11B	45
TX12A	12	TX12B	46
TX13A	13	TX13B	47
TX14A	14	TX14B	48
TX15A	15	TX15B	49
TX16A ²	16	TX16B ²	50
Ground ¹	17	Ground ¹	51
RX1A	18	RX1B	52
RX2A	19	RX2B	53

Signal	P2 Pin	Signal	P2 Pin
RX3A	20	RX3B	54
RX4A	21	RX4B	55
RX5A	22	RX5B	56
RX6A	23	RX6B	57
RX7A	24	RX7B	58
RX8A	25	RX8B	59
Ground ¹	26	Ground ¹	60
RX9A	27	RX9B	61
RX10A	28	RX10B	62
RX11A	29	RX11B	63
RX12A	30	RX12B	64
RX13A	31	RX13B	65
RX14A	32	RX14B	66
RX15A	33	RX15B	67
RX16A ²	34	RX16B ²	68

Notes:

- 1 The ground pins are provided for shielding, as required.
- 2 The ARINC 573/717 signals are supported on the respective channel 16 pins for both the BPRZ and HBP protocols. The selected protocol processed is based on the selection of the ARINC 717 HBP and BPRZ Encoding bits in the respective Transmit Channel Configuration register. See the API routine AR_SET_573_CONFIG for the method to define the ARINC 573/717 active encoding selection for this output pin.

Discrete and IRIG Input/Output Connector Pin-out

All RAR-PCIE product configurations have the same Discrete and IRIG I/O pin-out definition for the P3 IDC-50 I/O connector located at the rear of the board, pin-compatible with the CEI-520 and RCEI-530 IDC-50 Discrete I/O pin-out. Figure 14 shows the view facing the receptacles of the P3 IDC-50 I/O Connector.

To externally wrap Discrete I/O channels, connect the output pins to the respective input pins, DOUTn to DINn.

49	47	45	43	41	39	37	35	33	31	29	27	25	23	21	19	17	15	13	11	9	7	5	3	1
50	48	46	44	42	40	38	36	34	32	30	28	26	24	22	20	18	16	14	12	10	8	6	4	2

Figure 14. RAR-PCIE P3 IDC-50 I/O Connector

Table 29. RAR-PCIE P3 IDC-50 I/O Connections

Signal	P3 Pin	Signal	P3 Pin
DIN1	1	DOUT8	26
DIN2	2	DOUT9	27
DIN3	3	DOUT10	28
DIN4	4	DOUT11	29
DIN5	5	DOUT12	30
DIN6	6	DOUT13	31
DIN7	7	DOUT14	32
DIN8	8	DOUT15	33
DIN9	9	DOUT16	34
DIN10	10	Ground	35
DIN11	11	Ground	36
DIN12	12	IRIGRX+	37
DIN13	13	IRIGRX-	38
DIN14	14	IRIGTX	39
DIN15	15	Ground	40
DIN16	16	Ground	41
Ground	17	Ground	42
Ground	18	N/C	43
DOUT1	19	N/C	44
DOUT2	20	N/C	45
DOUT3	21	N/C	46
DOUT4	22	N/C	47
DOUT5	23	N/C	48
DOUT6	24	N/C	49
DOUT7	25	Ground	50

Note:

The ground pins are provided as Discrete I/O return lines or for shielding, as required.

IRIG-B Signal Connections

IRIG-B time (AM or DC/TTL) may be received via signals IRIGRX+ and IRIGRX- (see Table 29). The following IRIG formats are accepted:

Table 30. RAR-PCIE IRIG Signal Connections

Format	Modulation Frequency	Frequency/Resolution	Coded Expressions
B	0, 1	0, 2	0, 1, 2, 3

Upon power-up completion of the firmware program load, the RAR-PCIE initiates IRIG B002 (DC/TTL) transmission from the onboard IRIG encoder via the IRIGTX signal (see Table 29). The IRIGTX signal can source/sink 16 mA at valid TTL levels.

To externally wrap the IRIG generator to the IRIG receiver, connect the IRIGTX signal to IRIGRX+ input, and connect the IRIGRX- input to Ground.

RAR-XMC

Overview

The RAR-XMC card is a multiple-channel ARINC interface available in several configurations. When configured as the RAR-XMC-16P16, this product includes thirty-two ARINC 429 channels, (sixteen fixed receivers and sixteen software programmable transmit/receive channels), in an XMC form-factor. Configurations are available supporting various fixed ARINC 429 transmit/receive channel counts, ARINC 573/717, Avionics Discrete I/O, and IRIG time synchronization. Bus adapter options are also available for operating the RAR-XMC in native PCI Express and Thunderbolt 3 environments. For additional information related to operating the RAR-XMC in a Thunderbolt 3 environment refer to the “TB3-TO-CMC-LP Thunderbolt™ 3 Expansion Adapter User's Guide” that is included with the RAR-XMC-TB product and available in the CEI-x30-SW distribution *Documentation* folder. The latest version is available at https://www.abaco.com/TB3LP_guide.

RAR-XMC Specifications

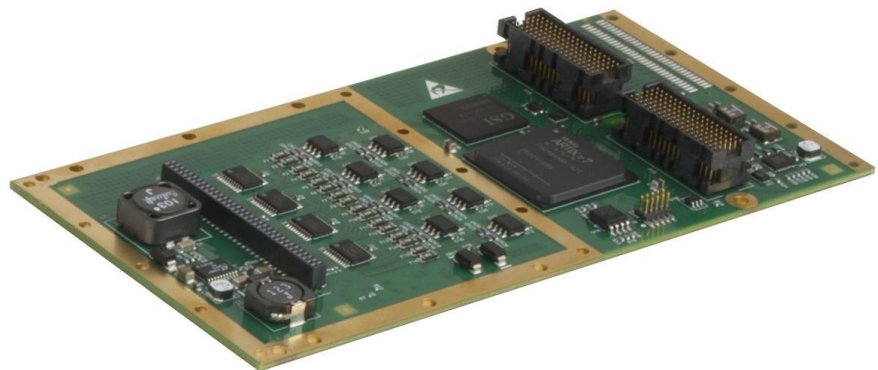


Figure 15. RAR-XMC

The RAR-XMC is a multiple channel, multiple protocol interface built to the XMC standards VITA 42.0/42.3, and IEEE-P1386.1.

PMC Express Interface

- XMC PCI Express Interface per the VITA 42.3-2006 standard

Transmit Channels

- Up to sixteen independent differential transmit channels
- Automatic parity generation
- 2048 message transmit buffer for each channel
- Baud rate/slew rate software-programmable for each channel
- Tri-state output capability
- 2048 entry message table supporting scheduled message transmission for all channels

Receiver Channels

- Up to thirty-two independent, differential receive channels
- 2048 message buffered mode receive buffer for each channel.
- 16384 message merged mode receive buffer
- Label/SDI message independent snapshot storage for each channel
- Independent merged/individual receive buffer operation.
- 64-bit, 1 μ sec resolution message time-tag
- Parity error detection

Software Programmable Transmit/Receive Channels

- Up to sixteen software programmable, differential transmit/receive channels, each having the characteristics of fixed transmit and receive channels as listed above.

Avionics Discrete Input and Output

- Four dedicated avionics-level discrete channels
- Output may switch to ground up to 500mA
- Power-up / reset default inactive
- Fixed input threshold of 2.0 +/- 0.2 volts

IRIG Input and Output

- IRIG-B Time-code receiver and transmitter

Typical Power Consumption

Table 31. RAR-XMC Power Consumption

+5V	+12V
800 mA	360 mA (no TX Loads)

Operating Temperature

-40 to +85 °C

Weight

3.6 ounces

PCI Memory Map

The following table summarizes the PCI memory map interface definition for the RAR-XMC.

Table 32. RAR-XMC PCI Memory Map

Region	Type	Size	Description
configuration	configuration	64 bytes	PCI configuration space
PCI BAR0	memory	512K bytes	RAR-XMC host interface
PCI BAR1	unused	0	not used
PCI BAR2	unused	0	not used
PCI BAR3	unused	0	not used
PCI BAR4	unused	0	not used
PCI BAR5	unused	0	not used

I/O Connections

RAR-XMC I/O Connector Designation

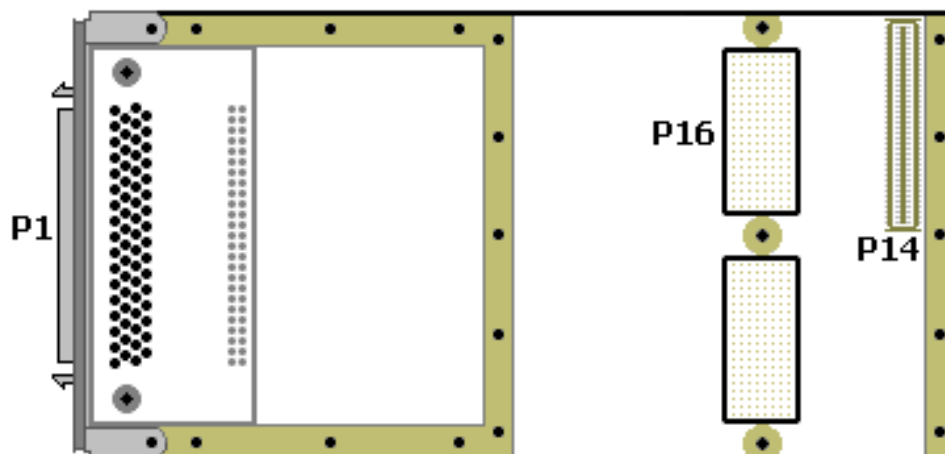


Figure 16. RAR-XMC I/O Connector Designation

Mating Connector

At publication of this document, the mating connector shown in Table 33 was compatible with the 68-pin SCSI-3 Front-Panel P1 connector used on the RAR-XMC. The Abaco Systems adapter cable CONSCSI3-6 is available for this connection.

Table 33. RAR-XMC P1 Front Panel I/O Mating Connector

Part No.	Description	Manufacturer
1-5750913-7	Front Panel 68 pin SCSI-3	AMP/Tyco

Input/Output Connector Pin-out

The different RAR-XMC product configurations have specific channel pin-out definitions based on the number of channels and protocols installed. ARINC 429 channels are supported in a reduced count for the “J” configuration ARINC 717 channels, and “N” configuration Discrete Input/Output connections.

Table 34 describes the pin-out for the optional P1 68-pin front panel connector and both the P16 (XMC) and optional P14 mezzanine I/O connectors. The pin-out may deviate slightly based on the hardware configuration of the RAR-XMC module. The exact channel pin-out

depends on the number of receivers and transmitters configured on your RAR-XMC.

Table 34. RAR-XMC Standard I/O Connections

Pin Designation	Signal	P1	P14	P16	Pin Designation	Signal	P1	P14	P16
CH1A	RX1A	1	63	A19	CH1B	RX1B	35	64	B19
CH2A	RX2A	2	61	F19	CH2B	RX2B	36	62	C19
CH3A	RX3A	3	59	D19	CH3B	RX3B	37	60	E19
CH4A	RX4A	4	57	F18	CH4B	RX4B	38	58	C18
CH5A	RX5A	5	55	A17	CH5B	RX5B	39	56	B17
CH6A	RX6A	6	53	F17	CH6B	RX6B	40	54	C17
CH7A	RX7A	7	51	D17	CH7B	RX7B	41	52	E17
CH8A	RX8A	8	49	F16	CH8B	RX8B	42	50	C16
CH9A	RX9A	9	47	A15	CH9B	RX9B	43	48	B15
CH10A	RX10A	10	45	F15	CH10B	RX10B	44	46	C15
CH11A	RX11A	11	43	D15	CH11B	RX11B	45	44	E15
CH12A	RX12A	12	41	F14	CH12B	RX12B	46	42	C14
CH13A	RX13A	13	39	A13	CH13B	RX13B	47	40	B13
CH14A	RX14A RX717A BPRZ ²	14	37	F13	CH14B	RX14B RX717B BPRZ ²	48	38	C13
CH15A DIN1	RX15A RX717A HBP ³ DIO INPUT 1 ⁴	15	35	D13	CH15B DIN2	RX15B RX717B HBP ³ DIO INPUT 2 ⁴	49	36	E13
CH16A DIN3	RX16A DIO INPUT 3 ⁴	16	N/A _{5,6}	N/A _{5,6}	CH16B DIN4	RX16B DIO INPUT 4 ⁴	50	N/A _{5,6}	N/A _{5,6}
CH17A	TX1A/RX17A	17	33	F12	CH17B	TX1B/RX17B	51	34	C12
CH18A	TX2A/ RX18A	18	31	A11	CH18B	TX2B/ RX18B	52	32	B11
CH19A	TX3A/RX19A	19	29	F11	CH19B	TX3B/RX19B	53	30	C11
CH20A	TX4A/RX20A	20	27	D11	CH20B	TX4B/ RX20B	54	28	E11
CH21A	TX5A/ RX21A	21	25	F10	CH21B	TX5B/ RX21B	55	26	C10
CH22A	TX6A/ RX22A	22	23	A9	CH22B	TX6B/ RX22B	56	24	B9
CH23A	TX7A/ RX23A	23	21	F9	CH23B	TX7B/ RX23B	57	22	C9
CH24A	TX8A/ RX24A	24	19	D9	CH24B	TX8B/ RX24B	58	20	E9
CH25A	TX9A/ RX25A	25	17	F8	CH25B	TX9B/ RX25B	59	18	C8
CH26A	TX10A/ RX26A	26	15	A7	CH26B	TX10B/ RX26B	60	16	B7
CH27A	TX11A/ RX27A	27	13	D7	CH27B	TX11B/ RX27B	61	14	E7
CH28A	TX12A/ RX28A	28	11	A5	CH28B	TX12B/ RX28B	62	12	B5
CH29A	TX13A/ RX29A	29	9	D5	CH29B	TX13B/ RX29B	63	10	E5
CH30A	TX14A/ RX30A TX717A ^{2,3}	30	7	A3	CH30B	TX14B/ RX30B TX717B BPRZ ²	64	8	B3
CH31A DOUT1	TX15A/ RX31A TX717B HBP ³ DIO OUTPUT 1 ⁴	31	5	D3	CH31B DOUT2	TX15B/ RX31B DIO OUTPUT 2 ⁴	65	6	E3
CH32A DOUT3	TX16A/ RX32A DIO OUTPUT 3 ⁴	32	N/A ⁵	N/A ⁵	CH32B DOUT4	TX16B/ RX32B DIO OUTPUT 4 ⁴	66	N/A ⁵	N/A ⁵
IRIGRX+	IRIGRX+	33	3	D1	IRIGRX-	IRIGRX-	67	4	E1
IRIGTX	IRIGTX	34	1	A1	GROUND	Ground ¹	68	2	E2

Notes:

Note 1: The ground pin is provided as a Discrete I/O return line or for shielding, as necessary.

Note 2: For the “J” configuration, the ARINC 717 BPRZ receive and transmit A/B signals are supported on these pins (replacing 429 signals).

Note 3: For the “J” configuration, the ARINC 717 HBP receive and transmit A/B signals are supported on these pins (replacing 429 signals).

Note 4: For the “N” configuration, only the Discrete Input and Output (DIO) connections are supported on these pins.

Note 5: The P14 and P16 mezzanine I/O connectors exclude connection to pins CH16A/B (DIN3/4), and CH32A/B (DOUT3/4).

Note 6: For the RAR-XMC-15P15 configuration only, CH16 (A/B signal pair for ARINC 429 Receive Channel 16) is included in the receiver configuration and total receiver count; however, it is not externally accessible or connected to any transmitter for the purpose of internal wrap. In the API fixed receivers are referenced as 0 through 14 and programmable channels as receivers are referenced as 16 through 31.

Figure 17 shows the view facing the receptacle of the 68-pin P1 Front-Panel (bezel) Connector (SCSI-3-compatible with Rails and Latch Blocks).

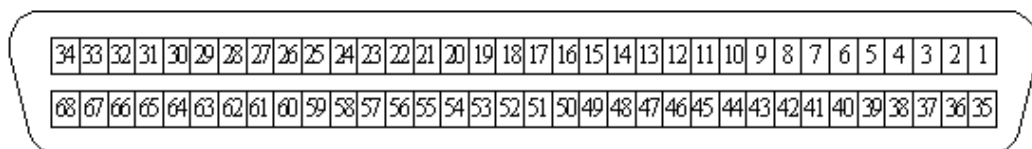


Figure 17. RAR-XMC P1 68-pin Front-Panel Connector

Optional RCONSCSI-N-D37-1 Adapter Cable

An optional adapter cable is available to provide a connection which is ARINC 429 and Discrete I/O pin-compatible with the RAR-EC/(R)CEI-715 adapter cables (CONRAR-EC, CONCEI-715, RCONCEI-715A), via the RCONSCSI-N-D37-1 (1320-109-8) cable.

RCONSCSI-N-D37-1 Adapter Cable Pin-out

The pin-out for the RCONSCSI-N-D37-1 Adapter Cable 37-pin D-Subminiature receptacle connector is shown below:



Figure 18. RCONSCSI-N-D37-1 Connector – View Facing Connector

Table 35. RCONSCSI-N-D37-1 Adapter Cable I/O Connections

Adapter Pin	SIGNAL	Adapter Pin	SIGNAL
1	RX1A	20	RX1B
2	RX2A	21	RX2B
3	RX3A	22	RX3B
4	RX4A	23	RX4B
5	RX5A	24	RX5B
6	RX6A	25	RX6B
7	RX7A	26	RX7B
9	RX8A	28	RX8B
10	TX1A	29	TX1B
11	TX2A	30	TX2B
12	TX3A	31	TX3B
13	TX4A	32	TX4B
14	Discrete I/O #1	33	Discrete I/O #2
15	Discrete I/O #3	34	Discrete I/O #4
17	Ground	36	Ground
18	IRIG TX	37	IRIG RX-
19	IRIG RX+		

Notes:

- 1 The ground pins are provided as Discrete I/O return lines or for shielding, as required.

IRIG-B Signal Connections

IRIG-B time (AM or DC/TTL) may be received via signals IRIGRX+ and IRIGRX- (see Table 34). The following IRIG formats are accepted.

Table 36. RAR-XMC IRIG Signal Formats

Format	Modulation Frequency	Frequency/Resolution	Coded Expressions
B	0, 1	0, 2	0, 1, 2, 3

Upon power-up completion of the firmware program load, the RAR-XMC initiates IRIG B002 (DC/TTL) transmission from the onboard IRIG encoder via the IRIGTX signal (see Table 34). The IRIGTX signal can source/sink 16 mA at valid TTL levels.

To externally wrap the IRIG generator to the IRIG receiver, connect the IRIGTX signal to IRIGRX+ input, and connect the IRIGRX- input to Ground.

Alternate P16 Rear Input/Output Connector Pin-out

Table 37 reflects the Rear-I/O connector pin-out for the fixed P16-only RAR-XMC configuration with 16 software programmable ARINC 429 channels, Discrete I/O, and IRIG (contact factory for availability).

Table 37. RAR-XMC Alternate P16-only I/O Connections

Pin Designation	Signal	P16	Pin Designation	Signal	P16
CH1A	TX1A/RX1A	A13	CH1B	TX1B/RX1B	B13
CH2A	TX2A/ RX2A	D15	CH2B	TX2B/ RX2B	E16
CH3A	TX3A/RX3A	E11	CH3B	TX3B/RX3B	E10
CH4A	TX4A/RX4A	E12	CH4B	TX4B/ RX4B	D11
CH5A	TX5A/ RX5A	D12	CH5B	TX5B/ RX5B	C11
CH6A	TX6A/ RX6A	B11	CH6B	TX6B/ RX6B	D19
CH7A	TX7A/ RX7A	A11	CH7B	TX7B/ RX7B	E13
CH8A	TX8A/ RX8A	D10	CH8B	TX8B/ RX8B	E14
CH9A	TX9A/ RX9A	D14	CH9B	TX9B/ RX9B	D13
CH10A	TX10A/ RX10A	E15	CH10B	TX10B/ RX10B	C13
CH11A	TX11A/ RX11A	B15	CH11B	TX11B/ RX11B	A15
CH12A	TX12A/ RX12A	A17	CH12B	TX12B/ RX12B	A19
CH13A	TX13A/ RX13A	E18	CH13B	TX13B/ RX13B	D17
CH14A	TX14A/ RX14A	B19	CH14B	TX14B/ RX14B	C15
CH15A	TX15A/ RX15A	C9	CH15B	TX15B/ RX15B	B9
CH16A	TX16A/ RX16A	A1	CH16B	TX16B/ RX16B	D9
DIN1	DISCRETE IN 1	D8	DOUT1	DISCRETE OUT 1	E4
DIN2	DISCRETE IN 2	D7	DOUT2	DISCRETE OUT 2	E5
DIN3	DISCRETE IN 3	E7	DOUT3	DISCRETE OUT 3	D6
DIN4	DISCRETE IN 4	E8	DOUT4	DISCRETE OUT 4	E6
IRIGRX+	IRIGRX+	F2	IRIGTX	IRIGTX	F3
GROUND	Ground ¹	F1	GROUND	Ground ¹	F4 - F19

Notes:

Note 1: The ground pins are provided as Discrete I/O return lines or for shielding, as necessary.

CEI-430

Overview

The CEI-430 card is a multiple-channel ARINC interface, available in several configurations for the PC/104-*Plus* platform. When configured as the CEI-430-1212, this card includes twenty-four ARINC 429 channels, (twelve receivers and twelve transmitters). There are many configurations available supporting various ARINC 429 channel counts, ARINC 573/717, Avionics Discrete I/O, Differential Discrete I/O, and IRIG time synchronization.

CEI-430 Specifications

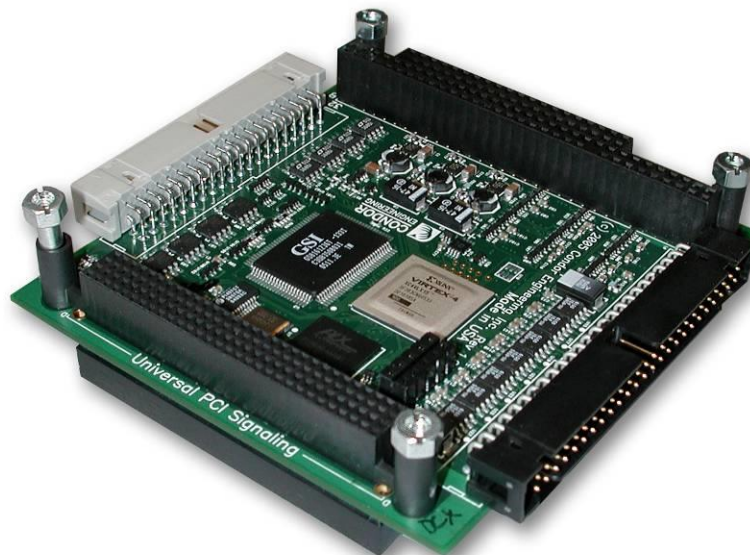


Figure 19. CEI-430

The CEI-430 is a multiple channel, multiple protocol interface built to the PC/104 Specification, version 2.5, PC/104-*Plus* Specification, version 2.0, and PCI-104 Specification, version 1.0.

PCI Interface

- Standard PCI Interface per the PCI Local Bus Specification Revision 2.2
- +5V and +3.3V PCI signaling compatibility and universal keying
- 33 MHz, 32-bit PCI operation

Note:

Per the PC/104-*Plus* Specification, the PCI Stack location of the CEI-430 is determined by card jumper shunts S0/S1. Refer to Table 38 for jumper mapping.

Table 38. CEI-430 PCI Stack Location Shunts

Stack Location	Installed Shunts	
	S1	S0
1	IN	IN
2	IN	OUT
3	OUT	IN
4	OUT	OUT

Transmit Channels

- Up to twelve independent differential serial transmit channels
- Automatic parity generation
- 2048 message transmit buffer for each channel
- Baud rate/slew rate software-programmable for each channel
- 2048 entry message table supporting scheduled message transmission for all channels

Receiver Channels

- Up to twelve independent, differential receive channels
- 2048 message buffered mode receive buffer for each channel
- 16384 message merged mode receive buffer
- Label/SDI message independent snapshot storage for each channel
- Independent merged/individual receive buffer operation
- 64-bit, 1 μ sec resolution message time-tag
- Parity error detection

Avionics Discrete Input and Output

- Up to sixteen bi-directional, avionics-level discrete channels
- Output may switch to ground up to 500mA
- Power-up / reset default inactive
- Fixed input threshold of 2.7 +/- 0.2 volts

Differential Discrete Input and Output

- Up to four RS-485 discrete channels
- Power-up / reset default inactive

IRIG Input and Output

- IRIG-B Time-code receiver and transmitter

Typical Power Consumption

Table 39. CEI-430 Power Consumption

5V	12V	-12V
300 mA	80 mA (no TX Loads) 200mA (twelve transmitters, maximum data rate, 400 Ω load each)	80 mA (no TX Loads) 200mA (twelve transmitters, maximum data rate, 400 Ω load each)

Operating Temperature

-40 to +85 °C

Weight

3.6 ounces, maximum

PCI Memory Map

The following table summarizes the PCI memory map interface definition for the CEI-430.

Table 40. CEI-430 PCI Memory Map

Region	Type	Size	Description
configuration	configuration	64 bytes	PCI configuration space
PCI BAR0	memory	128 bytes	PCI9030 memory-mapped local configuration registers
PCI BAR1	unused	0	PCI9030 I/O-mapped local configuration registers, unused
PCI BAR2	memory	512K bytes	CEI-430 host interface
PCI BAR3	unused	0	not used
PCI BAR4	unused	0	not used
PCI BAR5	unused	0	not used

I/O Connections

CEI-430 Outline Drawing

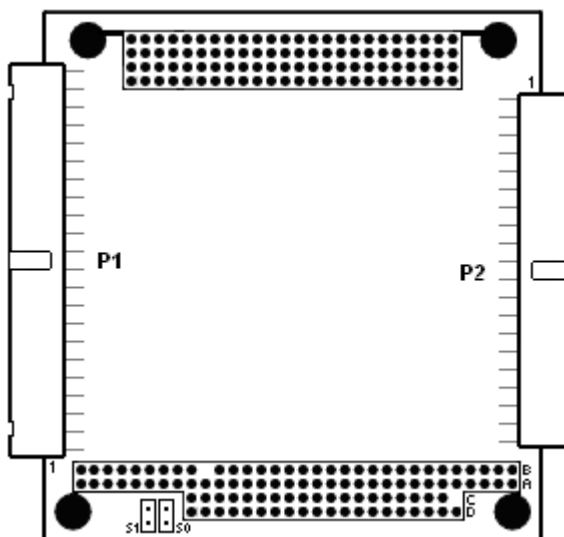


Figure 20. CEI-430 Outline Drawing

Input/Output Connectors

At publication of this document, the following mating connectors were compatible with the 50-pin (P1) and 40-pin (P2) IDC ribbon connectors used on the CEI-430. One each mating connector and retaining clip is provided for these connectors.

Table 41. CEI-430 Input/Output Connectors

Connector	Part No	Description	Manufacturer
P1	1-1658622-0	50 pin Ribbon 0.100 Centers	AMP/Tyco
	3425-6650	50 pin Ribbon 0.100 Centers	3M
P2	1-1658622-9	40 pin Ribbon 0.100 Centers	AMP/Tyco
	3417-6640	40 pin Ribbon 0.100 Centers	3M

Input/Output Connector Pin-out

Various CEI-430 product configurations have specific channel pin-out definitions based on the number of channels and protocols included. Table 42 describes the P1 connector pin layout for the CEI-430 module. The exact ARINC 429 channel pin-out depends on the number of receivers and transmitters configured on your CEI-430. Note that for the -J version of

the CEI-430, ARINC 573/717 protocol support replaces ARINC 429 Channel 12. Figure 21 shows the view facing the receptacles of the P1 IDC-50 ARINC I/O Connector.

To externally wrap ARINC signals, connect the transmitter signals to the respective receiver signals, TXnA to RXnA and TXnB to RXnB.

49	47	45	43	41	39	37	35	33	31	29	27	25	23	21	19	17	15	13	11	9	7	5	3	1
50	48	46	44	42	40	38	36	34	32	30	28	26	24	22	20	18	16	14	12	10	8	6	4	2

Figure 21. CEI-430 P1 50-pin IDC-50 ARINC Interface Connector

Table 42. CEI-430 P1 ARINC I/O Connections

Signal	P1 Pin	Signal	P1 Pin
RX1A	1	RX1B	2
RX2A	3	RX2B	4
RX3A	5	RX3B	6
RX4A	7	RX4B	8
RX5A	9	RX5B	10
RX6A	11	RX6B	12
RX7A	13	RX7B	14
RX8A	15	RX8B	16
RX9A	17	RX9B	18
RX10A	19	RX10B	20
RX11A	21	RX11B	22
RX12A ¹	23	RX12B ¹	24
Ground	25	Ground	26
TX1A	27	TX1B	28
TX2A	29	TX2B	30
TX3A	31	TX3B	32
TX4A	33	TX4B	34
TX5A	35	TX5B	36
TX6A	37	TX6B	38
TX7A	39	TX7B	40
TX8A	41	TX8B	42
TX9A	43	TX9B	44
TX10A	45	TX10B	46
TX11A	47	TX11B	48
TX12A ²	49	TX12B ²	50

Notes:

1. For –J configurations, the ARINC 573/717 protocol replaces ARINC 429 channel 12. The selected protocol processed is based on the selection of the ARINC 717 HBP and BPRZ Encoding bits in the respective Transmit Channel Configuration register. See the API routine AR_SET_573_CONFIG for the method to define the ARINC 573/717 active encoding selection for these output pins.
2. The ground pins are provided for shielding, as necessary

Figure 22 shows the view facing the receptacles of the P2 IDC-40 I/O Connector. Table 43 describes the P2 connector pin layout for the Discrete I/O, Differential I/O, and IRIG signals for the CEI-430.

39	37	35	33	31	29	27	25	23	21	19	17	15	13	11	9	7	5	3	1
40	38	36	34	32	30	28	26	24	22	20	18	16	14	12	10	8	6	4	2

Figure 22. CEI-430 P2 40-pin IDC-40 I/O Connector

Table 43. CEI-430 P2 I/O Connections

Signal	P2 Pin	Signal	P2 Pin
Ground	1	Ground	2
ADISC1	3	ADISC2	4
ADISC3	5	ADISC4	6
ADISC5	7	ADISC6	8
ADISC7	9	ADISC8	10
ADISC9	11	ADISC10	12
ADISC11	13	ADISC12	14
ADISC13	15	ADISC14	16
ADISC15	17	ADISC16	18
Ground	19	Ground	20
DIFF1+	21	DIFF1-	22
DIFF2+	23	DIFF2-	24
DIFF3+	25	DIFF3-	26
DIFF4+	27	DIFF4-	28
Ground	29	Ground	30
IRIGRX+	31	IRIGRX-	32
IRIGTX	33	GND	34
Reserved	35	Reserved	36
Reserved	37	Reserved	38
Reserved	39	Reserved	40

Note:

The ground pins are provided as Discrete I/O return lines or for shielding, as required.

IRIG-B Signal Connections

IRIG-B time (AM or DC/TTL) may be received via signals IRIGRX+ and IRIGRX- (see Table 43). The following IRIG formats are accepted:

Table 44. CEI-430 IRIG Signal Connections

Format	Modulation Frequency	Frequency/Resolution	Coded Expressions
B	0, 1	0, 2	0, 1, 2, 3

Upon completion of the program load, the CEI-430 initiates IRIG B002 (DC/TTL) transmission from the onboard IRIG encoder via the IRIGTX signal (see Table 43). The IRIGTX signal can source/sink 16 mA at valid TTL levels.

To externally wrap the IRIG generator to the IRIG receiver, connect the IRIGTX signal to IRIGRX+ input, and connect the IRIGRX- input to Ground.

CEI-430A

Overview

The CEI-430A card is a multiple-channel ARINC 429 interface version of the CEI-430 with an emphasis on high ARINC 429 receive channel count, designed for the PC/104-*Plus* platform. When configured as the CEI-430-2404, this card includes twenty-eight ARINC 429 channels, (twenty-four receivers and four transmitters), and Avionics Discrete I/O. Configurations are available with additional support for ARINC 573/717 and IRIG time synchronization.

CEI-430A Specifications



Figure 23. CEI-430A

The CEI-430A is a multiple channel, multiple protocol interface built to the PC/104 Specification, version 2.5, PC/104-*Plus* Specification, version 2.0, and PCI-104 Specification, version 1.0.

PCI Interface

- Standard PCI Interface per the PCI Local Bus Specification Revision 2.2
- +5V and +3.3V PCI signaling compatibility and universal keying
- 33 MHz, 32-bit PCI operation

Note:

Per the PC/104-*Plus* Specification, the PCI Stack location of the CEI-430A is determined by card jumper shunts S0/S1. Refer to Table 45 for jumper mapping.

Table 45. CEI-430A PCI Stack Location Shunts

Stack Location	Installed Shunts	
	S1	S0
1	IN	IN
2	IN	OUT
3	OUT	IN
4	OUT	OUT

Transmit Channels

- Two or four independent differential serial transmit channels
- Optional dedicated ARINC 573 / 717 transmit channel
- Automatic parity generation
- 2048 message transmit buffer for each channel
- Baud rate/slew rate software-programmable for each channel
- 2048 entry message table supporting scheduled message transmission for all channels

Receiver Channels

- Twenty-four independent, differential receive channels
- Optional dedicated ARINC 573 / 717 receive channel
- 2048 message buffered mode receive buffer for each channel
- 16384 message merged mode receive buffer
- Label/SDI message independent snapshot storage for each channel
- Independent merged/individual receive buffer operation
- 64-bit, 1 μ sec resolution message time-tag
- Parity error detection

Avionics Discrete Input and Output

- Sixteen bi-directional, avionics-level discrete channels
- Output may switch to ground up to 500mA
- Power-up / reset default inactive
- Fixed input threshold of 2.7 +/- 0.2 volts

IRIG Input and Output

- IRIG-B Time-code receiver and transmitter

Typical Power Consumption

Table 46. CEI-430A Power Consumption

5V
300 mA (no TX loads)
500 mA (four transmitters, 100KHz data rate, 400 Ω load each)

Operating Temperature

-40 to +85 °C

Weight

3.6 ounces, maximum

PCI Memory Map

The following table summarizes the PCI memory map interface definition for the CEI-430A.

Table 47. CEI-430A PCI Memory Map

Region	Type	Size	Description
configuration	configuration	64 bytes	PCI configuration space
PCI BAR0	memory	128 bytes	PCI9030 memory-mapped local configuration registers
PCI BAR1	unused	0	PCI9030 I/O-mapped local configuration registers, unused
PCI BAR2	memory	512K bytes	CEI-430A host interface
PCI BAR3	unused	0	not used
PCI BAR4	unused	0	not used
PCI BAR5	unused	0	not used

I/O Connections

CEI-430A Outline Drawing

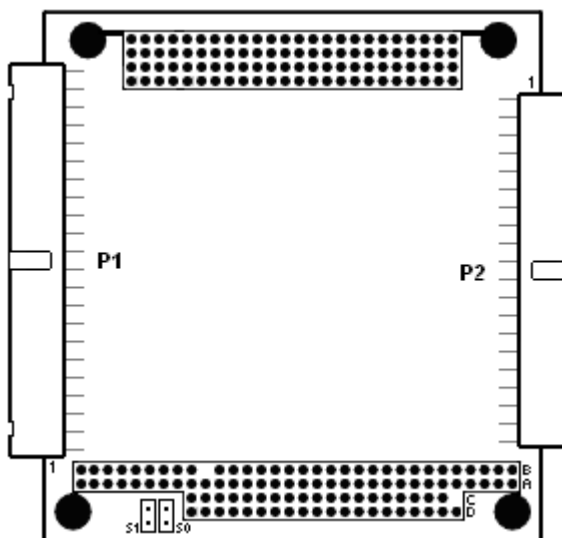


Figure 24. CEI-430A Outline Drawing

Input / Output Connectors

At publication of this document, the following mating connectors were compatible with the 50-pin (P1) and 40-pin (P2) IDC ribbon connectors

used on the CEI-430A. One each mating connector and retaining clip is provided for these connectors.

Table 48. CEI-430A Input/Output Connectors

Connector	Part No	Description	Manufacturer
P1	1-1658622-0	50 pin Ribbon 0.100 Centers	AMP/Tyco
	3425-6650	50 pin Ribbon 0.100 Centers	3M
P2	1-1658622-9	40 pin Ribbon 0.100 Centers	AMP/Tyco
	3417-6640	40 pin Ribbon 0.100 Centers	3M

Input / Output Connector Pin-out

Table 49 and Table 50 describe the connector pin layout for the CEI-430A module. The exact pin-out for the P2 connector depends on the number of ARINC 429 channels, ARINC 717 support, and IRIG support configured on your CEI-430A. Figure 25 shows the view facing the receptacles of the P1 IDC-50 I/O Connector. Figure 26 shows the view facing the receptacles of the P2 IDC-40 I/O Connector.

To externally wrap ARINC signals, connect the P2 transmitter signals to the respective receiver signals, TXnA to RXnA and TXnB to RXnB.

49	47	45	43	41	39	37	35	33	31	29	27	25	23	21	19	17	15	13	11	9	7	5	3	1
50	48	46	44	42	40	38	36	34	32	30	28	26	24	22	20	18	16	14	12	10	8	6	4	2

Figure 25. CEI-430A P1 50-pin IDC-50 Interface Connector

Table 49. CEI-430A P1 ARINC I/O Connections

Signal	P1 Pin	Signal	P1 Pin
RX1A	1	RX1B	2
RX2A	3	RX2B	4
RX3A	5	RX3B	6
RX4A	7	RX4B	8
RX5A	9	RX5B	10
RX6A	11	RX6B	12
RX7A	13	RX7B	14
RX8A	15	RX8B	16
RX9A	17	RX9B	18
RX10A	19	RX10B	20
RX11A	21	RX11B	22
RX12A	23	RX12B	24
Ground	25	Ground	26
RX13A	27	RX13B	28
RX14A	29	RX14B	30
RX15A	31	RX15B	32
RX16A	33	RX16B	34
RX17A	35	RX17B	36
RX18A	37	RX18B	38
RX19A	39	RX19B	40
RX20A	41	RX20B	42
RX21A	43	RX21B	44
RX22A	45	RX22B	46
RX23A	47	RX23B	48
RX24A	49	RX24B	50

Notes:

The ground pins are provided for shielding, as necessary

39	37	35	33	31	29	27	25	23	21	19	17	15	13	11	9	7	5	3	1
40	38	36	34	32	30	28	26	24	22	20	18	16	14	12	10	8	6	4	2

Figure 26. CEI-430A P2 40-pin IDC-40 I/O Connector**Table 50. CEI-430A P2 I/O Connections**

Signal	P2 Pin	Signal	P2 Pin
Ground	1	Ground	2
ADISC1	3	ADISC2	4
ADISC3	5	ADISC4	6
ADISC5	7	ADISC6	8
ADISC7	9	ADISC8	10
ADISC9	11	ADISC10	12
ADISC11	13	ADISC12	14
ADISC13	15	ADISC14	16
ADISC15	17	ADISC16	18
Ground	19	Ground	20
429TX1A	21	429TX1B	22
429TX2A	23	429TX2B	24
429TX3A	25	429TX3B	26
429TX4A	27	429TX4B	28
Ground	29	Ground	30
IRIGRX+	31	IRIGRX-	32
IRIGTX	33	GND	34
717RXA	35	717RXB	36
NC	37	717TXB	38
NC	39	717TXA	40

Note:

The ground pins are provided as Discrete I/O return lines or for shielding, as required.

Pins 37 and 39 have no connection.

IRIG-B Signal Connections

IRIG-B time (AM or DC/TTL) may be received via signals IRIGRX+ and IRIGRX- (see Table 50). The following IRIG formats are accepted:

Table 51. CEI-430A IRIG Signal Connections

Format	Modulation Frequency	Frequency/Resolution	Coded Expressions
B	0, 1	0, 2	0, 1, 2, 3

Upon completion of the program load, the CEI-430 initiates IRIG B002 (DC/TTL) transmission from the onboard IRIG encoder via the IRIGTX signal (see Table 50). The IRIGTX signal can source/sink 16 mA at valid TTL levels.

To externally wrap the IRIG generator to the IRIG receiver, connect the IRIGTX signal to IRIGRX+ input, and connect the IRIGRX- input to Ground.

AMC-A30

Overview

The AMC-A30 product line is a multiple-channel ARINC interface, available in several configurations. When configured as the AMC-A30-1414, this product includes twenty-eight ARINC 429 channels, (fourteen receivers and fourteen transmitters), in an AMC form-factor. There are a variety of configurations available supporting various ARINC 429 channel counts, ARINC 573/717, Avionics Discrete I/O, and IRIG time synchronization.

AMC-A30 Specifications



Figure 27. AMC-A30

The AMC-A30 is a multiple channel, multiple protocol interface built to the AMC.1 specification.

AMC/PCIe Interface

- Half-height, single-width AMC form factor
- AMC.1 compliant
- PCI Express (x4 lane) host interface

Transmit Channels

- Up to fourteen independent differential serial transmit channels
- Automatic parity generation
- 2048 message transmit buffer for each channel
- Baud rate/slew rate software-programmable for each channel
- 1024 entry message table supporting scheduled message transmission for all channels

Receiver Channels

- Up to fourteen independent, differential receive channels
- 2048 message buffered mode receive buffer for each channel.
- 16384 message merged mode receive buffer
- Label/SDI message independent snapshot storage for each channel
- Independent merged/individual receive buffer operation.
- 64-bit, 1 μ sec resolution message time-tag
- Parity error detection

Avionics Discrete Input and Output

- Four bi-directional, avionics-level discrete channels
- Output may switch to ground up to 500mA
- Fixed input threshold of 2.7 +/- 0.2 volts

IRIG Input and Output

- IRIG-B Time-code receiver and transmitter

Typical Power Consumption

Table 52. AMC-A30 Payload Power Consumption

+12V
370 mA (no TX Loads)

Operating Temperature

-40 to +85 °C

Weight

4.8 ounces

PCI Memory Map

The following table summarizes the PCI memory map interface definition for the AMC-A30.

Table 53. AMC-A30 PCI Memory Map

Region	Type	Size	Description
configuration	configuration	64 bytes	PCI configuration space
PCI BAR0	memory	512 bytes	PCI9056 memory-mapped local configuration registers
PCI BAR1	I/O	256 bytes	PCI9056 I/O-mapped local configuration registers, unused
PCI BAR2	memory	512K bytes	AMC-A30 host interface
PCI BAR3	unused	0	not used
PCI BAR4	unused	0	not used
PCI BAR5	unused	0	not used

I/O Connections

Input/Output Connectors

At publication of this document, the following mating connector was compatible with the 100-pin Micro-D connector used on the AMC-A30.

Table 54. AMC-A30 Input/Output Connectors

Part No.	Description	Manufacturer
MWDM2L-100PSS	100-pin Micro-D Connector	Glenair

Input/Output Connector Pin-out

The different AMC-A30 product configurations have specific channel pin-out definitions based on the number of channels and protocols installed. Table 55 describes the 100-pin front panel for the ARINC 429 version of the AMC-A30 module. The exact ARINC 429 channel pin-out depends on the number of receivers and transmitters configured on your AMC-A30. Table 56 describes the pin-out differences for the -J version of the AMC-A30; these pins support ARINC 573/717 protocols on the pins used by the upper channels on non-J configurations.

To externally wrap ARINC signals, connect the transmitter signals to the respective receiver signals, TXnA to RXnA and TXnB to RXnB.

Table 55. AMC-A30 I/O Connections

Signal	Pin	Signal	Pin	Signal	Pin
Reserved	1	TX10B	35	Reserved	69
Gnd (note)	2	TX8B	36	RX7A	70
Reserved	3	TX7B	37	Reserved	71
Discrete 4	4	TX5B	38	RX4A	72
Reserved	5	TX4B	39	Reserved	73
TX12B	6	TX2B	40	RX1A	74
Reserved	7	TX1B	41	Reserved	75
TX9B	8	Discrete 2	42	Reserved	76
Reserved	9	RX14B	43	Reserved	77
TX6B	10	RX12B	44	Reserved	78
Reserved	11	RX11B	45	IRIGRX+	79
TX3B	12	RX9B	46	Gnd (note)	80
Reserved	13	RX8B	47	TX14A	81
Gnd (note)	14	RX6B	48	TX13A	82
Reserved	15	RX5B	49	TX11A	83
RX13B	16	RX3B	50	TX10A	84
Reserved	17	RX2B	51	TX8A	85
RX10B	18	IRIG_TX	52	TX7A	86
Reserved	19	Reserved	53	TX5A	87
RX7B	20	Discrete 3	54	TX4A	88
Reserved	21	Reserved	55	TX2A	89
RX4B	22	TX12A	56	TX1A	90
Reserved	23	Reserved	57	Discrete 1	91
RX1B	24	TX9A	58	RX14A	92
Reserved	25	Reserved	59	RX12A	93
Reserved	26	TX6A	60	RX11A	94

Signal	Pin	Signal	Pin	Signal	Pin
Reserved	27	Reserved	61	RX9A	95
Reserved	28	TX3A	62	RX8A	96
Reserved	29	Reserved	63	RX6A	97
IRIGRX-	30	Gnd (note)	64	RX5A	98
Gnd (note)	31	Reserved	65	RX3A	99
TX14B	32	RX13A	66	RX2A	100
TX13B	33	Reserved	67		
TX11B	34	RX10A	68		

Note:

The ground pins are provided as Discrete I/O return lines or for shielding, as necessary.

Table 56. AMC-A30-xxxx-J I/O Connection for ARINC 573/717

Signal	Pin	Signal	Pin	Signal	Pin
ARINC 717 BPRZ TXB	6	Reserved	43	Reserved	81
ARINC 717 HBP RXB	16	ARINC 717 BPRZ RXB	44	ARINC 717 HBP TXB	82
Reserved	32	ARINC 717 TXA (note)	56	Reserved	92
Reserved	33	ARINC 717 HBP RXA	66	ARINC 717 BPRZ RXA	93

Note:

The ARINC 573/717 TXA (High) signal is supported on this pin for both the BPRZ and HBP protocols. The selected protocol processed is based on the selection of the ARINC 717 HBP and BPRZ Encoding bits in the respective Transmit Channel Configuration register. See the API routine AR_SET_573_CONFIG for the method to define the ARINC 573/717 active encoding selection for this output pin.

IRIG-B Signal Connections

IRIG-B time (AM or DC/TTL) may be received via signals IRIGRX+ and IRIGRX- (see Table 55). The following IRIG formats are accepted:

Table 57. IRIG Signal Formats

Format	Modulation Frequency	Frequency/Resolution	Coded Expressions
B	0, 1	0, 2	0, 1, 2, 3

Upon completion of the program load, the AMC-A30 initiates IRIG B002 (DC/TTL) transmission from the onboard IRIG encoder via the IRIGTX signal (see Table 55). The IRIGTX signal can source/sink 16 mA at valid TTL levels.

To externally wrap the IRIG generator to the IRIG receiver, connect the IRIGTX signal to IRIGRX+ input, and connect the IRIGRX- input to Ground.

RAR-EC

Overview

The RAR-EC card is a multiple-channel ARINC interface, available in several configurations for the ExpressCard form factor. When configured as a RAR-EC-74, this card includes eleven ARINC 429 channels, (seven receivers and four transmitters). There are a variety of configurations available supporting various ARINC 429 channel counts, ARINC 573/717, Avionics Discrete I/O, and IRIG time synchronization.

RAR-EC Specifications



Figure 28. RAR-EC

The RAR-EC is a multiple channel, multiple protocol interface built to the ExpressCard Specification, Release 1.2.

ExpressCard Interface

- PCI-Express Interface per the PCI Local Bus Specification Revision 2.2
- 54 mm ExpressCard format

Transmit Channels

- Up to four independent differential serial transmit channels
- Automatic parity generation
- 2048 message transmit buffer for each channel
- Baud rate/slew rate software-programmable for each channel
- 2048 entry message table supporting scheduled message transmission for all channels

Receiver Channels

- Up to seven independent, differential receive channels
- 2048 message buffered mode receive buffer for each channel
- 16384 message merged mode receive buffer
- Label/SDI message independent snapshot storage for each channel
- Independent merged/individual receive buffer operation
- 64-bit, 1 μ sec resolution message time-tag
- Parity error detection

Avionics Discrete Input and Output

- Up to four bi-directional, avionics-level discrete channels
- Output may switch to ground up to 500mA
- Power-up / reset default inactive
- Fixed input threshold of 2.7 +/- 0.2 volts

IRIG Input and Output

- IRIG-B Time-code receiver and transmitter

Typical Power Consumption

Table 58. RAR-EC Power Consumption

+3.3V	1.5V
750 mA	0mA

Operating Temperature

-40 to +85 °C

Weight

TBD ounces, maximum

PCI Memory Map

The following table summarizes the PCI memory map interface definition for the RAR-EC.

Table 59. RAR-EC PCI Memory Map

Region	Type	Size	Description
configuration	configuration	64 bytes	PCI configuration space
PCI BAR0	memory	128 bytes	PCI9030 memory-mapped local configuration registers
PCI BAR1	unused	0	PCI9030 I/O-mapped local configuration registers, unused
PCI BAR2	memory	512K bytes	RAR-EC host interface
PCI BAR3	unused	0	not used
PCI BAR4	unused	0	not used
PCI BAR5	unused	0	not used

I/O Connections

Mating Connectors

At publication of this document, the following mating connector was compatible with the Champ36 connector provided on the RAR-EC enclosure end-plate. Abaco Systems supplies the adapter cable CONAREC-30 or CONAREC-180 for this connection.

Table 60. RAR-EC P1 Input/Output Connector

Connector	Part No	Description	Manufacturer
P1	2-5175677-5	Champ 36	AMP/Tyco
P1	0543063619	Champ 36	Molex

ARINC Input/Output Connector Pin-out

Various RAR-EC product configurations have specific channel pin-out definitions based on the number of channels and protocols included. Table 61 describes the P1 connector pin layout for the RAR-EC, while Table 62 describes the adapter cable connector pin-out. The exact ARINC 429 channel pin-out depends on the number of receivers and transmitters configured on your RAR-EC. Note that for the -J version of the RAR-EC, ARINC 573/717 protocol support replaces the receive channel 7 and transmit channel 4 ARINC 429 A and B I/O pins.

To externally wrap ARINC signals, connect the transmitter signals to the respective receiver signals, TXnA to RXnA and TXnB to RXnB.

Table 61. RAR-EC P1 ARINC I/O Connections

Signal	P1 Pin	Signal	P1 Pin
RX1A	1	RX1B	19
RX2A	2	RX2B	20
RX3A	3	RX3B	21
RX4A	4	RX4B	22
RX5A	5	RX5B	23
RX6A	6	RX6B	24
RX7A ²	7	RX7B ²	25
TX1A	8	TX1B	26
TX2A	9	TX2B	27
TX3A	10	TX3B	28
TX4A ²	11	TX4B ²	29
Discrete I/O 1	12	Discrete I/O 2	30
Discrete I/O 3	13	Discrete I/O 4	31
IRIG RX+	14	IRIG RX-	32
IRIG TX	15	Ground ¹	33
Reserved	16	Ground ¹	34
Reserved	17	Reserved	35
Reserved	18	Reserved	36

Notes:

- 1 The ground pins are provided as Discrete I/O return lines or for shielding, as required.
- 2 The ARINC 573/717 signals are supported on the respective transmit channel 4 and receive channel 7 pins for both the BPRZ and HBP protocols. The selected transmit protocol processed is based on the selection of the ARINC 717 HBP and BPRZ Encoding bits in the respective Transmit Channel Configuration register. See the API routine AR_SET_573_CONFIG for the method to define the ARINC 573/717 active encoding selection for this output pin.

Transition Cable Pin-out

An adapter cable is provided to transition from the 36 pin device I/O connector to a 37-pin Subminiature D receptacle connector, with the pin-out shown in Table 62 below. Figure 29 shows the view facing the receptacles of the RAR-EC Transition Cable I/O Connector.

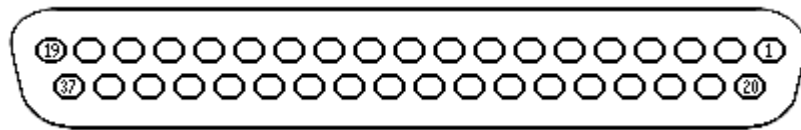


Figure 29. RAR-EC Transition Cable Connector

Table 62. RAR-EC-XX Transition Cable Connections

Adapter Pin-out	SIGNAL	Adapter Pin-out	SIGNAL
1	RX1A	20	RX1B
2	RX2A	21	RX2B
3	RX3A	22	RX3B
4	RX4A	23	RX4B
5	RX5A	24	RX5B
6	RX6A	25	RX6B
7	RX7A	26	RX7B
8	Reserved	27	Reserved
9	Reserved	28	Reserved
10	TX1A	29	TX1B
11	TX2A	30	TX2B
12	TX3A	31	TX3B
13	TX4A	32	TX4B
14	Discrete I/O 1	33	Discrete I/O 2
15	Discrete I/O 3	34	Discrete I/O 4
16	Reserved	35	Reserved
17	Ground	36	Ground
18	IRIG TX	37	IRIG RX-

Adapter Pin-out	SIGNAL	Adapter Pin-out	SIGNAL
19	IRIG RX+		

Notes:

- 1 The ground pins are provided as Discrete I/O return lines or for shielding, as required.
- 2 The ARINC 573/717 signals are supported on their transmit channel 4 and receive channel 7 pins for both the BPRZ and HBP protocols. The selected transmit protocol processed is based on the selection of the ARINC 717 HBP and BPRZ Encoding bits in the respective Transmit Channel Configuration register. See the API routine AR_SET_573_CONFIG for the method to define the ARINC 573/717 active encoding selection for this output pin.

IRIG-B Signal Connections

IRIG-B time (AM or DC/TTL) may be received via signals IRIGRX+ and IRIGRX-. The following IRIG formats are accepted:

Table 63. RAR-EC IRIG Signal Connections

Format	Modulation Frequency	Frequency/Resolution	Coded Expressions
B	0, 1	0, 2	0, 1, 2, 3

Upon completion of the program load, the RAR-EC initiates IRIG B002 (DC/TTL) transmission from the onboard IRIG encoder via the IRIGTX signal. The IRIGTX signal can source/sink 16 mA at valid TTL levels.

To externally wrap the IRIG generator to the IRIG receiver, connect the IRIGTX signal to IRIGRX+ input, and connect the IRIGRX- input to Ground.

RAR-CPCI

Overview

The RAR-CPCI card is a multiple-channel ARINC interface, available in several configurations for the CompactPCI platform. When configured as a RAR-CPCI-1616, this card includes thirty-two ARINC 429 channels, (sixteen receivers and sixteen transmitters). There are a variety of configurations available supporting various ARINC 429 channel counts, ARINC 573/717, Avionics Discrete I/O, and IRIG time synchronization.

RAR-CPCI Specifications



Figure 30. RAR-CPCI

The RAR-CPCI is a multiple channel, multiple protocol interface built to the PICMG 2.0 Revision 3 CompactPCI® Specification, PXI™ Specification Revision 2.0, and PXI™ Hardware Specification Revision 2.1.

PCI Interface

- Standard PCI Interface per the PCI Local Bus Specification Revision 2.2
- +5V and +3.3V PCI signaling compatibility and universal keying
- 66 MHz, 32-bit PCI operation

Transmit Channels

- Up to sixteen independent differential serial transmit channels
- Automatic parity generation
- 2048 message transmit buffer for each channel
- Baud rate/slew rate software-programmable for each channel
- 2048 entry message table supporting scheduled message transmission for all channels

Receiver Channels

- Up to sixteen independent, differential receive channels
- 2048 message buffered mode receive buffer for each channel
- 16384 message merged mode receive buffer
- Label/SDI message independent snapshot storage for each channel
- Independent merged/individual receive buffer operation
- 64-bit, 1 µsec resolution message time-tag
- Parity error detection

Avionics Discrete Input and Output

- Sixteen bi-directional, avionics-level discrete channels
- Output may switch to ground up to 500mA
- Power-up / reset default inactive
- Fixed input threshold of 2.7 +/- 0.2 volts

IRIG Input and Output

- IRIG-B Time-code receiver and transmitter

Typical Power Consumption

Table 64. RAR-CPCI Power Consumption

+3.3V	5V	+12V	-12V
500 mA	50 mA	100 mA (no TX Loads) 350mA (sixteen transmitters, max data rate, 400Ω load each)	100 mA (no TX Loads) 350mA (sixteen transmitters, max data rate, 400Ω load each)

Operating Temperature

-40 to +85 °C

Weight

3.6 ounces, maximum

PCI Memory Map

The following table summarizes the PCI memory map interface definition for the RAR-CPCI.

Table 65. RAR-CPCI PCI Memory Map

Region	Type	Size	Description
configuration	configuration	64 bytes	PCI configuration space
PCI BAR0	memory	512 bytes	PCI9056 memory-mapped local configuration registers
PCI BAR1	I/O	256 bytes	PCI9056 I/O-mapped local configuration registers, unused
PCI BAR2	memory	512K bytes	RAR-CPCI host interface
PCI BAR3	unused	0	not used
PCI BAR4	unused	0	not used
PCI BAR5	unused	0	not used

I/O Connections

RAR-CPCI Outline Drawing

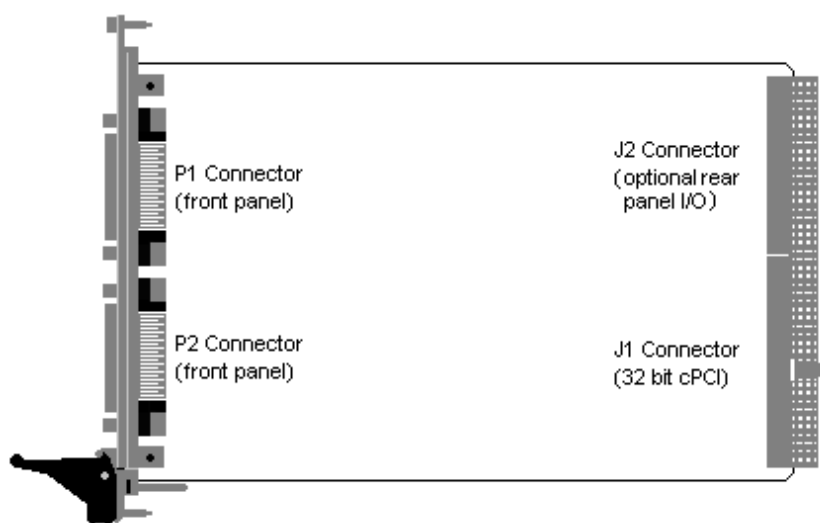


Figure 31. RAR-CPCI Outline Drawing

Mating Connectors

At publication of this document, the following mating connector was compatible with the 50-pin (P1 and P2) Champ connectors provided on the RAR-CPCI front panel (bezel). Abaco Systems supplies the adapter cable CONCEI-620 for this connection.

Table 66. RAR-CPCI P1/P2 Input/Output Connectors

Connector	Part No	Description	Manufacturer
P1 and P2	787131-1	Front Panel 50 pin Champ	AMP/Tyco

ARINC Input/Output Connector Pin-out

Various RAR-CPCI product configurations have specific channel pin-out definitions based on the number of channels and protocols included.

Table 67 describes the P1/P2 connector pin layout for the RAR-CPCI. The exact ARINC 429 channel pin-out depends on the number of receivers and transmitters configured on your RAR-CPCI. For the -J version of the RAR-CPCI, the ARINC 573/717 protocol support pins replace the channel 16 ARINC 429 I/O pins. Note the RAR-CPCI I/O connections are not pin-compatible with the CEI-620.

Use the Compact-PCI J2 back plane connector to couple the RAR-CPCI to ARINC devices and discrete inputs/outputs for rear panel configurations, (see Table 68). For front panel configurations, two connectors, P1 and P2, are provided. Each connector is identical. Figure 32 shows the view facing the receptacles of the P1/P2 AMP Champ 0.8mm Front Panel (bezel) ARINC I/O Connectors.

To externally wrap ARINC signals, connect the transmitter signals to the respective receiver signals, TXnA to RXnA and TXnB to RXnB.

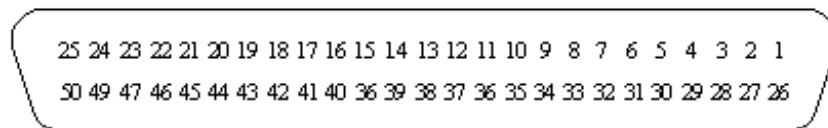


Figure 32. RAR-CPCI P1/P2 50-pin Front-Panel I/O Connectors

Table 67. RAR-CPCI P1/P2 Front Panel I/O Connections

P1 Connector						P2 Connector					
Pin	D50	Signal	Pin	D50	Signal	Pin	D50	Signal	Pin	D50	Signal
1	1	TX1A	26	34	TX1B	1	1	TX9A	26	34	TX9B
2	18	TX2A	27	2	TX2B	2	18	TX10A	27	2	TX10B
3	35	TX3A	28	19	TX3B	3	35	TX11A	28	19	TX11B
4	3	TX4A	29	36	TX4B	4	3	TX12A	29	36	TX12B
5	20	TX5A	30	4	TX5B	5	20	TX13A	30	4	TX13B
6	37	TX6A	31	21	TX6B	6	37	TX14A	31	21	TX14B
7	5	TX7A	32	38	TX7B	7	5	TX15A	32	38	TX15B
8	22	TX8A	33	6	TX8B	8	22	TX16A ²	33	6	TX16B ²
9	39	RX1A	34	23	RX1B	9	39	RX9A	34	23	RX9B
10	7	RX2A	35	40	RX2B	10	7	RX10A	35	40	RX10B
11	24	RX3A	36	8	RX3B	11	24	RX11A	36	8	RX11B
12	41	RX4A	37	25	RX4B	12	41	RX12A	37	25	RX12B
13	9	RX5A	38	42	RX5B	13	9	RX13A	38	42	RX13B
14	26	RX6A	39	10	RX6B	14	26	RX14A	39	10	RX14B
15	43	RX7A	40	27	RX7B	15	43	RX15A	40	27	RX15B
16	11	RX8A	41	44	RX8B	16	11	RX16A ²	41	44	RX16B ²
17	28	Ground ¹	42	12	Ground ¹	17	28	Ground ¹	42	12	Ground ¹
18	45	IRIGRX+	43	29	IRIGRX-	18	45	IRIGRX+	43	29	IRIGRX-
19	13	IRIGTX	44	46	Ground	19	13	IRIGTX	44	46	Ground
20	30	Ground ¹	45	14	Ground ¹	20	30	Ground ¹	45	14	Ground ¹
21	47	Ground ¹	46	31	Ground ¹	21	47	Ground ¹	46	31	Ground
22	15	Discrete IO 1	47	48	Discrete IO 2	22	15	Discrete IO 9	47	48	Discrete IO 10
23	32	Discrete IO 3	48	16	Discrete IO 4	23	32	Discrete IO 11	48	16	Discrete IO 12
24	49	Discrete IO 5	49	33	Discrete IO 6	24	49	Discrete IO 13	49	33	Discrete IO 14
25	17	Discrete IO 7	50	50	Discrete IO 8	25	17	Discrete IO 15	50	50	Discrete IO 16

Notes:

- 1 The ground pins are provided as Discrete I/O return lines or for shielding, as required.
- 2 The ARINC 573/717 signals are supported on the respective channel 16 pins for both the BPRZ and HBP protocols. The selected protocol processed is based on the selection of the ARINC 717 HBP and BPRZ Encoding bits in the respective Transmit Channel Configuration register. See the API routine AR_SET_573_CONFIG for the method to define the ARINC 573/717 active encoding selection for this output pin.

Table 68. RAR-CPCI Rear Panel Input/Output Connector Definition

	Row a	Row b	Row c	Row d	Row e
1		TX9B	TX9A	TX1B	TX1A
2		TX10B	TX10A	TX2B	TX2A
3		TX11B	TX11A	TX3B	TX3A
4		TX12B	TX12A	TX4B	TX4A
5		TX13B	TX13A	TX5B	TX5A
6		TX14B	TX14A	TX6B	TX6A
7		TX15B	TX15A	TX7B	TX7A
8		TX16B	TX16A	TX8B	TX8A
9		RX9B	RX9A	RX1B	RX1A
10		RX10B	RX10A	RX2B	RX2A
11		RX11B	RX11A	RX3B	RX3A
12	Ground ¹	RX12B	RX12A	RX4B	RX4A
13	IRIGTX	RX13B	RX13A	RX5B	RX5A
14	IRIGRX-	RX14B	RX14A	RX6B	RX6A
15	IRIGRX+	RX15B	RX15A	RX7B	RX7A
16		RX16B	RX16A	RX8B	RX8A
17					
18					
19	Discrete IO 13				
20	Discrete IO 14	Discrete IO 10	Discrete IO 7	Discrete IO 4	Discrete IO 1
21	Discrete IO 15	Discrete IO 11	Discrete IO 8	Discrete IO 5	Discrete IO 2
22	Discrete IO 16	Discrete IO 12	Discrete IO 9	Discrete IO 6	Discrete IO 3

Notes:

1 Per the compact PCI specification, row "A" is closest to the edge of the circuit board and Row "E" is furthest from the edge of the circuit board.

2 The ground pins are provided as Discrete I/O return lines or for shielding, as required.

IRIG-B Signal Connections

IRIG-B time (AM or DC/TTL) may be received via signals IRIGRX+ and IRIGRX-. The following IRIG formats are accepted:

Table 69. RAR-CPCI IRIG Signal Connections

Format	Modulation Frequency	Frequency/Resolution	Coded Expressions
B	0, 1	0, 2	0, 1, 2, 3

On completion of the program load, the RAR-CPCI initiates IRIG B002 (DC/TTL) transmission from the onboard IRIG encoder via the IRIGTX signal. The IRIGTX signal can source/sink 16 mA at valid TTL levels.

To externally wrap the IRIG generator to the IRIG receiver, connect the IRIGTX signal to IRIGRX+ input, and connect the IRIGRX- input to Ground.

RAR15-XMC

Overview

The RAR15-XMC product line consists of XMC form-factor modules with multiple protocols and channel configurations, including both MIL-STD-1553 and ARINC. Products in this line include the RAR15-XMC-FIO/RAR15XF (front I/O) and RAR15-XMC-IT/RAR15X (rear I/O).

The pin assignments and module specifications are defined in the “MIL-STD-1553 Hardware Installation Manual (1500-046)”.

The programming and operation of MIL-STD-1553 functionality is documented in the following manuals:

- “BusTools/1553-API Software User’s Manual (1500-045)”
- “BusTools/1553-API UCA Reference Manual (1500-038)”
- “MIL-STD-1553 Enhanced Universal Core Architecture (UCA32) Global Register & Memory Map Reference Manual”
- “MIL-STD-1553 Enhanced Universal Core Architecture (UCA32) Local Processing Unit (LPU) Reference Manual”.

Special considerations for multi-protocol boards

Host Memory Map

Dedicated ARINC-only boards covered in this manual use a single 512Kbyte PCI BAR0 memory region for the host interface. Multi-protocol boards share a single PCI BAR0 memory region with MIL-STD-1553 UCA host interface. On multi-protocol boards, all ARINC functions are still programmed in a single 512Kbyte region, but this region is offset from the beginning of the PCI BAR0 region by 1 Megabyte (see the

chapter “CEI-x30 Hardware Interface” for a detailed description of the CEI-x30 ARINC 512 Kbyte host interface).

Discrete I/O

On multi-protocol boards, the MIL-STD-1553 interface controls the discrete I/O. For this reason, all multi-protocol boards will report to the host via the ARINC registers that no discrete I/O is supported.

IRIG-B

On multi-protocol boards, the MIL-STD-1553 interface controls the IRIG-B interface. For this reason, all multi-protocol boards will report to the host via the ARINC registers that IRIG is not supported. IRIG-relative time-stamp synchronization is achieved as described below.

Time-stamp Synchronization

Although all ARINC receive messages are time-stamped with an internal 64-bit, one microsecond, dedicated ARINC timer, receive messages may still be correlated to time relative to any of the MIL-STD-1553 channels. Each MIL-STD-1553 channel uses an independent timer which may be synchronized to IRIG-B, an external clock, or operate internally. See the *Timer Registers* and *Multi-protocol Timer Registers* sections in the chapter “CEI-x30 Hardware Interface” for a description of the various timer read registers. These registers contain the simultaneously latched values of the internal ARINC timer as well as the timers from each MIL-STD-1553 channel. Having simultaneous sample values for each timer allows the host software to calculate time for ARINC receive messages relative to each of the various time-stamp domains.

See the paragraph titled *Receive Message Time-tagging and Timer Usage* in the “CEI-x30 Product Features” chapter of this document, for a more detailed description on how to perform time-stamp synchronization between the ARINC 429 received message processing and MIL-STD-1553 channel timers.

Source File Build Options

When compiling the CEI-x30 API source files for an embedded target operating system with RAR15-XMC products, define the directive `FLASH_BASED_TARGET` to omit the other CEI-x30 board firmware load modules from the resulting compilation of `CDEV_API.C`.

RCEI-830X820

Overview

The RCEI-830X820 card is a multiple-channel ARINC 429 interface available in optional channel configurations, designed to replicate the CEI-820 rear-I/O pin-out. When configured as the RCEI-830X820-88, this product includes sixteen ARINC 429 channels, (eight receivers and eight transmitters), in a PMC form-factor. A variety of bus adapter configurations are also available, supporting both front and rear-I/O access for PCI, PCI Express, and CompactPCI platforms.

RCEI-830X820 Specifications

The RCEI-830X820 is a multiple channel ARINC 429 interface built to the PMC standard IEEE-P1386.1.

PMC/PCI Interface

- Standard single-width CMC module per IEEE-P1386.1 draft standard
- +5V and +3.3V PCI signaling compatibility and universal keying
- 66 MHz, 32-bit PCI operation

Transmit Channels

- Up to eight independent differential serial transmit channels
- Automatic parity generation
- 2048 message transmit buffer for each channel
- Baud rate/slew rate software-programmable for each channel

- 2048 entry message table supporting scheduled message transmission for all channels

Receiver Channels

- Up to eight independent, differential receive channels
- 2048 message buffered mode receive buffer for each channel.
- 16384 message merged mode receive buffer
- Label/SDI message independent snapshot storage for each channel
- Independent merged/individual receive buffer operation.
- 64-bit, 1 μ sec resolution message time-tag
- Parity error detection

Typical Power Consumption

Table 70. RCEI-830X820 Power Consumption

+3.3V	+5V	+12V	-12V
500 mA	50 mA	100 mA (no TX Loads)	100 mA (no TX Loads)

Operating Temperature

-40 to +85 °C

Weight

3.6 ounces

PCI Memory Map

The following table summarizes the PCI memory map interface definition for the RCEI-830X820.

Table 71. RCEI-830X820 PCI Memory Map

Region	Type	Size	Description
configuration	configuration	64 bytes	PCI configuration space
PCI BAR0	memory	512 bytes	PCI9056 memory-mapped local configuration registers

Region	Type	Size	Description
PCI BAR1	I/O	256 bytes	PCI9056 I/O-mapped local configuration registers, unused
PCI BAR2	memory	512K bytes	RCEI-830X820 host interface
PCI BAR3	n/a	0	not used
PCI BAR4	n/a	0	not used
PCI BAR5	n/a	0	not used

I/O Connections

Front Input /Output Connector

The RCEI-830X820 front-I/O connector type and pin-out match the CEI-830 front-panel 68-pin SCSI-3 pin-out (see Table 6), for ARINC 429 signals RX and TX 1-8. The RCEI-830X820 P14 mezzanine I/O connector pin-out does not match the CEI-830; rather, the rear I/O pin-out is designed to match the CEI-820 P14 pin assignments.

Rear Input/Output Connector Pin-out

The RCEI-830X820 product configurations have specific channel pin-out definitions based on the number of ARINC 429 channels installed. Table 72 describes the P14 mezzanine I/O connector pin-out for the RCEI-830X820 module. The exact ARINC 429 channel pin-out depends on the number of receivers and transmitters configured on your RCEI-830X820.

To externally wrap ARINC signals, connect the transmitter signals to the respective receiver signals, TXnA to RXnA and TXnB to RXnB.

Table 72. RCEI-830X820 P14 I/O Connections

Signal	P14 I/O Connector	Signal	P14 I/O Connector
N/C	1	N/C	2
N/C	3	N/C	4
N/C	5	N/C	6
N/C	7	N/C	8
TX8A	9	TX8B	10
TX7A	11	TX7B	12
TX6A	13	TX6B	14
TX5A	15	TX5B	16
TX4A	17	TX4B	18
TX3A	19	TX3B	20
TX2A	21	TX2B	22
TX1A	23	TX1B	24
RX8A	25	RX8B	26
RX7A	27	RX7B	28
RX6A	29	RX6B	30
RX5A	31	RX5B	32
RX4A	33	RX4B	34
RX3A	35	RX3B	36
RX2A	37	RX2B	38
RX1A	39	RX1B	40
GND	41	GND	42
N/C	43	N/C	44
N/C	45	N/C	46
GND	47	GND	48
N/C	49	N/C	50
N/C	51	N/C	52
N/C	53	N/C	54
N/C	55	N/C	56
N/C	57	N/C	58
N/C	59	N/C	60
N/C	61	N/C	62
N/C	63	N/C	64

Note:

The ground pins are provided as Discrete I/O return lines or for shielding, as necessary.

RAR-MPCIE

Overview

The RAR-MPCIE card is a multiple-channel ARINC 429 interface available in optional channel configurations, designed for the embedded mini-PCI Express form-factor. When configured as the RAR-MPCIE-84, this product includes twelve ARINC 429 channels, (eight receivers and four transmitters), with four bidirectional discrete channels and IRIG-B. Optional configurations support ARINC 717 transmission and reception. A bus adapter configuration is also available supporting host access via full-height single-lane PCI Express.

RAR-MPCIE Specifications



Figure 33. RAR-MPCIE

The RAR-MPCIE is a multiple channel ARINC 429 interface built to the PCI Express Mini Card Electromechanical Specification, Revision 2.0.

PCI Express Interface

- Standard PCI Express Interface per the PCI Express Base Specification, Revision 2.0

Transmit Channels

- Up to four independent differential serial transmit channels
- Automatic parity generation
- 2048 message transmit buffer for each channel
- Baud rate/slew rate software-programmable for each channel
- 2048 entry message table supporting scheduled message transmission for all channels

Receiver Channels

- Up to eight independent, differential receive channels
- 2048 message buffered mode receive buffer for each channel.
- 16384 message merged mode receive buffer
- Label/SDI message independent snapshot storage for each channel
- Independent merged/individual receive buffer operation.
- 64-bit, 1 μ sec resolution message time-tag
- Parity error detection

Avionics Discrete Input and Output

- Four dedicated avionics-level discrete channels
- Output may switch to ground up to 200mA
- Power-up / reset default inactive
- Fixed input threshold of 2.0 +/- 0.2 volts

IRIG Input and Output

- IRIG-B Time-code receiver and transmitter

Typical Power Consumption

Power measurements taken with four transmitters actively transmitting at 100Kbps into a 400 Ω load.

Table 73. RAR-MPCIE Power Consumption

+3.3V aux	-1.2V
450mA	0mA

Operating Temperature

-40 to +85 °C

Weight

Approximately 0.305 oz (8.6g)

PCI Memory Map

The following table summarizes the PCI memory map interface definition for the RAR-MPCIE.

Table 74. RAR-MPCIE PCI Memory Map

Region	Type	Size	Description
configuration	configuration	64 bytes	PCI configuration space
PCI BAR0	memory	512K bytes	RAR-MPCIE host interface
PCI BAR1	n/a	0	not used
PCI BAR2	n/a	0	not used
PCI BAR3	n/a	0	not used
PCI BAR4	n/a	0	not used
PCI BAR5	n/a	0	not used

I/O Connections

Input/Output Connectors

Various RAR-MPCIE product configurations have specific channel pin-out definitions based on the number of channels and protocols included.

Two I/O connector options are available with the RAR-MPCIE product, a 37-pin rugged nano-D connector (J1), and a 50-pin SlimStack 0.4mm pitch flexible cable connector (J2).

Table 75. RAR-MPCIE Input/Output Connectors

Connector	Part No	Description	Manufacturer
J1	A39100-837	37-pin rugged nano-D	Omnetics
J2	503304-5040	50-pin SlimStack 0.4mm	Molex

Table 76 describes the connector pin-out both connector options. The exact ARINC 429 channel pin-out depends on the number of receivers and transmitters configured on your RAR-MPCIE. For the -J version of the RAR-MPCIE, the ARINC 573/717 protocol support pins replace the respective RX8A/B ARINC 429 Receiver I/O pins and TX4A/B ARINC 429 Transmitter I/O pins.

Table 76. RAR-MPCIE I/O Connections

Signal	Rugged Connector	Molex Connector	Signal	Rugged Connector	Molex Connector
RX1A	1	37	RX1B	20	12
RX2A	2	38	RX2B	21	13
RX3A	3	39	RX3B	22	14
RX4A	4	40	RX4B	23	15
RX5A	5	43	RX5B	24	18
RX6A	6	44	RX6B	25	19
RX7A	7	45	RX7B	26	20
2.5V	8	30	TCK	27	8
RX8A - RX717A ²	9	46	RX8B - RX717B ²	28	21
TX1A	10	47	TX1B	29	22
TX2A	11	48	TX2B	30	23
TX3A	12	49	TX3B	31	24
TX4A - TX717A ²	13	50	TX4B - TX717B ²	32	25
Discrete I/O 1	14	29	Discrete I/O 2	33	4
Discrete I/O 3	15	34	Discrete I/O 4	34	9
TDI	16	31	TDO	35	6
TMS	17	7	Ground ¹	36	10, 11, 28, 32, 33, 35, 36
IRIGTX	18	1	IRIGRX-	37	27
IRIGRX+	19	26	3.3V	N/C	5
Chassis	38, 39	16, 17, 41, 42			

Notes:

- 1 The ground pins are provided as Discrete I/O return lines or for shielding, as required.
- 2 For the two "J" configurations, the ARINC 717 BPRZ and HBP receive and transmit A/B signals are supported on these pins (replacing the respective ARINC 429 signals).

To externally wrap ARINC signals, connect the transmitter signals to the respective receiver signals, TXnA to RXnA and TXnB to RXnB.

Optional Adapter Cables

Two optional adapter cables are available to provide easy access to the RAR-MPCIE I/O connectors. The D-Sub37 adapter end of both cables supports a connection which is ARINC 429 and Discrete I/O pin-compatible with the RAR-EC/(R)CEI-715 adapter cables (CONRAR-EC, CONCEI-715, RCONCEI-715A), and the RAR-USB adapter cable (RCONRARUSB-EC).

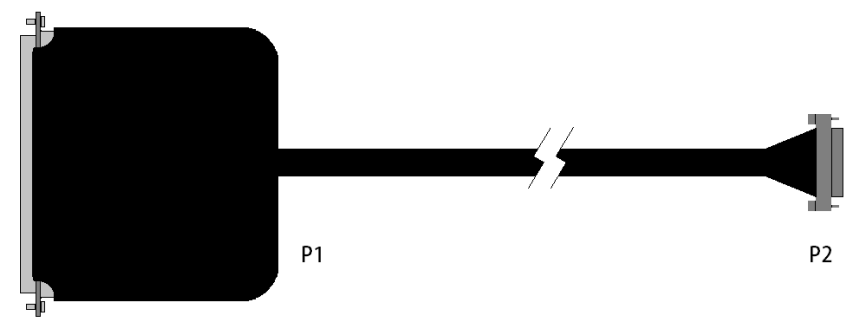


Figure 34. RAR-MPCIE Rugged Adapter Cable

Adapter Cable Pin Orientation

The pin orientation for both Adapter Cable 37-pin D-Subminiature receptacle connectors is shown below, view facing the connector:



Figure 35. RAR-MPCIE Adapter Cable P1 Connector – View Facing

Adapter Cable Pin-Out

Table 77 describes the pin-out for the Adapter Cable 37-pin D-Subminiature receptacle connector P1.

Table 77. RAR-MPCIE Adapter Cable P1 I/O Connections

Adapter Pin	SIGNAL	Adapter Pin	SIGNAL
1	RX1A	20	RX1B
2	RX2A	21	RX2B
3	RX3A	22	RX3B
4	RX4A	23	RX4B

Adapter Pin	SIGNAL	Adapter Pin	SIGNAL
5	RX5A	24	RX5B
6	RX6A	25	RX6B
7	RX7A	26	RX7B
8	No Connect	27	No Connect
9	RX8A ²	28	RX8B ²
10	TX1A	29	TX1B
11	TX2A	30	TX2B
12	TX3A	31	TX3B
13	TX4A ³	32	TX4B ³
14	Discrete #1	33	Discrete #2
15	Discrete #3	34	Discrete #4
16	No Connect	35	No Connect
17	Ground	36	Ground
18	IRIG TX	37	IRIG RX-
19	IRIG RX+		

Notes:

- 1 The ground pins are provided as Discrete I/O return lines or for shielding, as required.
- 2 For the two "J" configurations, the ARINC 573/717 receive signals are supported on the respective channel 8 (RX8A/RX8B) pins for both the BPRZ and HBP protocols.
- 3 For the two "J" configurations, the ARINC 573/717 transmit signals are supported on the respective channel 4 (TX4A/TX4B) pins for both the BPRZ and HBP protocols.

IRIG-B Signal Connections

IRIG-B time (AM or DC/TTL) may be received via signals IRIGRX+ and IRIGRX-. The following IRIG formats are accepted:

Table 78. RAR-MPCIE IRIG Signal Connections

Format	Modulation Frequency	Frequency/Resolution	Coded Expressions
B	0, 1	0, 2	0, 1, 2, 3

CEI-x30 Product Features

Overview

The CEI-x30 products provide specialized features for receive message storage and time-tagging, timer usage, and transmit message scheduling. The following paragraphs document several of these features, and how they might be used in your ARINC application.

Enhanced CEI-x30 Interface

Beginning with the release of CEI-x30-SW Version 2.00 (firmware version 3), all CEI-x30 products provide enhanced features, including full exposure of all channel register sets to the host PCI interface, time-stamped Snapshot Buffer message storage, and Filter Table triggered hardware interrupt support. This enhanced feature set includes a larger firmware host interface, requiring a modification to the default PCI BAR2 memory definition stored in an onboard EEPROM for older boards. The process by which an older CEI-x30 device EEPROM BAR2 size attribute is modified is handled via AR_SET_DEVICE_CONFIG API routine invocation with the *item* parameter ARU_HW_ENHANCE_UPDATE.

ARINC 429 Software Programmable Transmit/Receive Channels

With the RAR-XMC ARINC board and (R)AR15-XMC multiprotocol boards, software programmable ARINC 429 transmit/receive channels were introduced. These ARINC 429 transmit and receive channels share the same I/O pins, and the function of ARINC 429 transmission or reception on those pins is controlled via the *Transmit Disable Bit* and the opposing states of the respective Channel Configuration Register 1 *Channel Enable Bit* for the receive and transmit channels assigned to those I/O pins. With the *Transmit Disable Bit* set and the *Transmitter Channel Enable Bit* clear, a software programmable channel with the assigned

Receiver *Channel Enable Bit* set will function as an ARINC 429 receive channel. With the Receiver *Channel Enable Bit* clear, a software programmable channel with the assigned Transmitter *Channel Enable Bit* set and *Transmit Disable Bit* clear functions as an ARINC 429 transmit channel. Having both receive and transmit functions enabled will result in the assigned receive channel receiving and buffering each transmitted ARINC 429 message. For products supporting software programmable channels, all programmable transmit channel outputs are initialized to, and remain in a tri-stated condition upon execution of the API initialization routine AR_OPEN. The application must explicitly program all transmitter *Transmit Disable Bit* values to the desired setting prior to the invocation of active message processing to enable external message transmission.

Controlling the state of the *Transmit Disable Bit* is performed using the AR_SET_DEVICE_CONFIG API routine with the ARU_TX_DISABLE option; control of individual channel transmission or reception is provided using the AR_SET_DEVICE_CONFIG API routine with the ARU_TX_FIFO_ENABLE and ARU_RX_FIFO_ENABLE options, respectively. The AR_SET_DEVICE_CONFIG API routine provides a single invocation to assign the software programmable channel pair state using the ARU_CONFIG_PROGRAMMABLE_CHAN option.

ARINC 429 Transmitter Tri-State Control

While all CEI-x30 products can support internal wrap of ARINC 429 messages without exposing the communications to a connected device, select CEI-x30 products have the capability to tri-state the output pins of transmit channels.

For most CEI-x30 products, the *Transmit Disable Bit* in the ARINC 429 Transmit Channel Configuration Register 1 only disables message transmission to the external bus, but does not prohibit the transmit circuit from driving a NULL voltage level at the I/O connector pin. The RAR-PCIE, RAR-MPCIE, RAR-XMC, RCEI-830X820 and RAR15-XMC multiprotocol products provide the ability to tri-state the transmitter output at the I/O connector pin using the *Transmit Disable Bit*, allowing any device connected to the respective I/O pins to drive ARINC 429 levels on the same bus with no adverse effect. On products with transmitter output tri-state capability, the outputs drive the respective transmit lines low until disabled by the host application.

ARINC 429 Protocol Support

Several aspects of the ARINC 429 protocol are handled by the CEI-x30 products.

The electrical transmission of ARINC 429 data over the bus is performed with the label field in reverse bit order. The transmit logic of the CEI-x30 product automatically reverses the bit order of the ARINC 429 message label (B0-B7) prior to transmission. The receiver logic of the CEI-x30 also reverses the bit order of the ARINC 429 message label prior to placing the data in the respective receive buffers. This ARINC 429 label modification is fixed in the CEI-x30 processing and cannot be modified by the application. For more information on the ARINC 429 protocol, see the document “ARINC Tutorial”.

ARINC 429 message parity is defined in the MSB of the ARINC 429 message. The CEI-x30 transmission logic provides the capability to generate either odd or even parity based on the bit states of the first 31 bits of the ARINC 429 message. When disabled, the transmitter logic transmits the message with the parity bit unaltered. When enabled, the firmware overwrites the value of the parity bit in the 32-bit user-defined message with the calculated parity value.

The CEI-x30 reception logic provides the capability to detect the parity of ARINC 429 messages based on the bit states within the message. When disabled, the receiver logic provides the received ARINC 429 message as it was received, (without modification). If enabled, the receiver logic modifies the state of the parity bit (B32) to be “0” if the parity was detected as odd and “1” if the parity was detected to be even.

The bus speed for both ARINC 429 transmission and reception may be programmed to any baud rate from 3.9Kbps to 800Kbps; however, the transmitted signal slew rate doesn’t provide for a good signal beyond 150Kbps.

The API routine `AR_SET_DEVICE_CONFIG` provides the method to set the transmit and receive channel bus speed and parity options for your device.

ARINC 585 Protocol Support

Support for 24-bit ARINC 585 2-wire and similar protocols is provided with the latest CEI-x30 firmware. This protocol does not support a standard ARINC 429 label field; instead it is transmitted as an unmodified 24-bit value, with the most significant 8 bits of the transmit buffer entry ignored.

ARINC 585 message parity is defined in the MSB of the 24-bit message. The CEI-x30 transmission logic provides the capability to generate either odd or even parity based on the bit states of the first 23 bits of the message. When disabled, the transmitter logic transmits the message with the parity bit unaltered. When enabled, the firmware overwrites the value of the parity bit in the 24-bit host-defined message with the calculated parity value.

The CEI-x30 reception logic provides the capability to detect the parity of ARINC 585 messages based on the bit states within the message. When disabled, the receiver logic provides the received message as it was received, (without modification). If enabled, the receiver logic modifies the state of the parity bit (MSB - B24) to be “0” if the parity was detected as odd and “1” if the parity was detected to be even.

ARINC 573/717 Protocol Support

Several aspects of the ARINC 573/717 HBP and BPRZ protocols are handled by the CEI-x30 products.

The electrical transmission of ARINC 573/717 data over the bus is performed at various bus speed/sub-frame size combinations resulting in the standard four-second frame duration. Each frame consists of four sub-frames comprised of a sub-frame sync word and subsequent data words. Each sync and data word is 12 bits long, transmitted in LSB-MSB order.

The transmit logic of a CEI-x30 board relies on the application to supply the frame data in a 16-bit unsigned integer array in which only the lower 12 bits of each 16-bit element are used. The application must supply the applicable sub-frame sync words and data in the respective locations within this array for proper frame transmission.

The receiver logic of a CEI-x30 board supports both raw and auto-synchronized frame data reception. With raw data frame data reception, the data captured and provided to the application is organized in the least significant 12-bits of each element of a 16-bit unsigned integer array, based on the first detected bit transition. With auto-synchronized frame data reception, four application-provided sub-frame sync words are used by the CEI-x30 ARINC 717 receive logic to synchronize reception and data logging to a detected sub-frame sequence. The sub-frame detection is based both on the provided sub-frame sync word bit patterns and the specified sub-frame size.

The API routine `AR_SET_573_CONFIG` provides the method to set transmit and receive channel bus speed and frame size options for your device.

CEI-x30 Timers

The CEI-x30 products support two independent timers, a 64-bit one-microsecond timer and an optional IRIG timer. The one-microsecond timer is utilized for all ARINC 429 receive message time-tagging. It can be assigned to any 64-bit value by the host at any time.

Specified in microseconds from January 1st of the current year, received IRIG time is based on an external IRIG-B reference connected to the IRIG-B input of the CEI-x30 device (see the section, “IRIG-B Signal Connections” for the procedure to connect the CEI-x30” device to the IRIG source). If the IRIG time reference is desired, but no external IRIG source is available, the CEI-x30 IRIG generator may be internally wrapped and used as the time source (see the ARU_IRIG_WRAP_ENABLE option of AR_SET_DEVICE_CONFIG); however, if the CEI-x30 IRIG generator is to be used by other data collection hardware in your system, it is best to externally connect the CEI-x30 device IRIG-B output to its IRIG-B input. The CEI-x30 IRIG-B generator can be reset by the host application to any desired value using the standard IRIG time format, (see AR_SET_TIME).

A user-programmable compensation to the CEI-x30 IRIG time value can be defined when a consistent offset to the IRIG source time value is desired. This compensation should be used when a consistent skew in IRIG time-tagging is encountered between ARINC 429 events occurring on the CEI-x30 and other IRIG time-tagged components in your system. This offset can be specified via the ARU_IRIG_SET_BIAS option of AR_SET_DEVICE_CONFIG.

An IRIG DAC threshold adjustment procedure is provided that configures the CEI-x30 device IRIG receiver for optimal signal reception. This procedure is usually not necessary; however, it may be required if IRIG timing appears unstable from a known good source.

First, test the stability of the IRIG signal by invoking AR_GET_DEVICE_CONFIG with the option ARU_IRIG_CALIBRATED. If this invocation returns a FALSE status, the adjustment should be invoked through use of the AR_SET_CONFIG routine with the ARU_IRIG_QUICK_ADJUSTMENT option. If the quick DAC adjustment is not successful, a more thorough adjustment may be performed. This adjustment is invoked through the ARU_IRIG_ADJUST_THRESHOLD option of the AR_SET_DEVICE_CONFIG routine. Execution of this IRIG adjustment may require at least one minute and should be performed only during the initialization of the board.

In addition to IRIG-B reception, CEI-x30 products can be configured to generate IRIG time using on-board IRIG-B circuitry. The transmitted IRIG time value is initialized to the host calendar time by the API, and can be modified by the host application via AR_SET_TIME.

Receive Message Time-tagging and Timer Usage

The CEI-x30 products time-stamp ARINC 429 received messages in the respective receive buffer and in the snapshot buffer (with label-only snapshot storage enabled), with a 64-bit one-microsecond time-tag. This

time-tag value is based on the on-board timer, recorded at approximately 1.5 bit times after the last bit of the 32-bit message is detected. The CEI-x30 API supports multiple time-tag reference methods based on this one-microsecond timer. The active timer reference mode may be assigned by the host application by invoking the API routine `AR_SET_DEVICE_CONFIG`, using the `ARU_RX_TIMETAG_MODE` option and the selections discussed below. Alternatively, the receive message API routines that support the `timeTag` structure parameter (`AR_GET*_XT`) allow the application to specify the time-tag format on an individual invocation basis via the `timeTag` structure member `timeTagFormat`. This assignment determines the format of the timer/time-tag value returned from all API invocations providing time-related information.

The following receive message time-tag and timer-read reference modes are available for selection:

IRIG 64-Bit Time Reference

This time reference is based on the CEI-x30 IRIG receiver, with the one-second resolution extrapolated by the one-microsecond internal timer to provide an estimated one-microsecond IRIG reference value. When the IRIG time reference is selected, all legacy receive data API routines based on a 32-bit time-tag parameter return a time-tag value with a resolution of one millisecond; while all receive data API routines supporting a 64-bit time-tag will return an IRIG timer-based time-tag.

The CEI-x30 device records the internal timer value when the IRIG signal is received and decoded, (referred to as IRIG Reference Time). The API then calculates the offset between the IRIG Reference Time and the received ARINC data time-tag. Finally, the API applies that offset to the IRIG signal time value to produce an IRIG-reference message time stamp for the received data, extrapolated to provide the 1 microsecond resolution.

Internal 64-Bit One Microsecond Time Reference

This time reference is based on the CEI-x30 device one-microsecond timer. When this mode is active, all legacy receive data API routines based on a 32-bit time-tag and all routines based on a 64-bit time-tag return a time-tag value with a resolution of one microsecond. The 32-bit time-tag is returned as the lower 32-bits of the 64-bit time-tag. This internal timer can be reset by the host application to any value desired, (see `AR_SET_TIME`).

Internal 32-Bit Twenty Microsecond Time Reference

This time reference is provided for backward compatibility to applications designed around the CEI-710 or IP-429HD-based products. When this mode is active, all legacy receive data API routines based on a 32-bit time-tag return a time-tag value with a resolution of twenty microseconds; all receive data API routines based on a single 64-bit time-tag value return a 32-bit value with a resolution of twenty microseconds (the upper 32-bits of the time-tag is zero).

Internal 32-Bit One Millisecond Time Reference

This time reference is based on a scaled version of the CEI-x30 device one-microsecond timer. When this mode is active, all legacy receive data API routines based on a 32-bit time-tag/timer value return a 32-bit value with a resolution of one millisecond; all receive data API routines based on a 64-bit time-tag/timer value return a 64-bit value with a resolution of one millisecond.

CEI-x20 Compatible Time Reference

This time-tag and timer option is not available as a selection via AR_SET_CONFIG/ ARU_RX_TIMETAG_MODE; instead, this time reference mode is selected when the CEI-x20 legacy API routine AR_SET_TIMERRATE is invoked. In this mode, time references are based on a programmable time-tag resolution specified through AR_SET_TIMERRATE. When this mode is active, all receive data API routines return a time-tag/timer value based on either a 32-bit or 64-bit value scaled using the application-defined resolution. The message rate and start offset attributes assigned to scheduled message table entries are also scaled to the application-defined resolution.

MIL-STD-1553 64-Bit Time Reference

Available only with the multi-protocol MIL-STD-1553/ARINC 429 products, this time reference is based on a synchronization between the ARINC 429 timer/time-stamp and the selected MIL-STD-1553 channel timer. When this timing mode is selected, all legacy receive data API routines based on a 32-bit time-tag parameter return a 1553-synchronized time-tag value with a resolution of one millisecond; while all receive data API routines supporting a 64-bit time-tag will return a 1553-timer synchronized value with a 1 nanosecond resolution.

In this timing mode, the CEI-x30 API records the internal timer-based time-stamp value logged when the specified MIL-STD-1553 channel timer value is read. The API then calculates the offset between the logged

channel time-stamp value and the received ARINC data time-tag. Finally, the API applies that offset to the MIL-STD-1553 channel timer value to produce a 1553-referenced message time stamp for the received data.

MIL-STD-1553 synchronized time-stamp string conversion is supported by the API routine `AR_CONVERT_1553_TIME_TO_STRING`.

Receive Message Buffering Methods

The CEI-x30 products provide three methods of message storage for receiving ARINC 429 data.

Individual Circular Buffer Storage

The first storage method is the individual circular buffer, (sometimes referred to as a sequential or FIFO buffer), in which ARINC 429 messages are continuously saved in the order in which they are received. Each receiver can store up to 2048 messages in its individual circular buffer before overflowing.

Note:

A transition of the Receive Buffer Enable from disabled to enabled will cause the receive buffer to reset, and all received messages stored therein will be lost.

Merged Circular Buffer Storage

The second storage method is the merged circular buffer. This buffer provides for time-based sequentially ordered receive message buffering for multiple receive channels in a single buffer. Each receiver can be individually enabled for storage in the merged circular buffer; however, message storage in the merged buffer is exclusive of the individual receive buffers. The merged circular buffer can store up to 16384 messages before overflowing.

It is important to note that once a buffer overflows, all messages previously contained therein are lost. For this reason, when using either of these circular buffer storage methods for data retrieval, the host application should periodically flush the buffers. The API routines `AR_GETWORD*`, `AR_GETNEXT*`, `AR_GET_DATA*`, and `AR_GET_BLOCK*` are provided to support various data retrieval methods for receive circular buffer storage.

Snapshot Buffer Storage

The third storage method is a snapshot buffer, sometimes referred to as dedicated storage. Independent of either circular buffer storage method, snapshot storage records the latest received message for each ARINC 429 Label and optional SDI field value combination on every receive channel. The API routine `AR_SET_DEVICE_CONFIG` should be invoked using the receive channel attribute `ARU_ACCESS_SNAPSHOT_BUFFER` to assign the snapshot storage mode based on the label field value alone or the combined label/SDI field values.

When the snapshot storage mode is configured to store messages based on the label field value alone, a 64-bit one microsecond time-tag is also recorded in the buffer with each message.

Prior to receiving a message with a specific label/SDI combination, the table is initialized to zero.

The API routines `AR_GET_LATEST` (message only) and `AR_GET_LATEST_T` (message with time-tag) should be invoked to retrieve ARINC 429 data from the snapshot buffer when the snapshot storage mode is set to *Label Only*; use `AR_GET_SNAP_DATA` when the storage mode is set to *Label and SDI*. Any zero value data retrieved from this buffer using either routine is an indication that the respective message has not been received on that channel.

Interrupts and Triggers

There are two interrupt and trigger sources available with the CEI-x30 products. Any event that can cause a trigger can also invoke a hardware interrupt on the PCI bus. For simplicity of discussion, the term “interrupt event” applies to both interrupts and triggers for the remainder of this section regardless of whether or not an actual hardware interrupt is generated as a result.

The mechanism by which an interrupt event is logged is the interrupt queue. The interrupt queue is a 2048 entry circular buffer, consisting of a single 32-bit value for each generated interrupt event. The most recent entry written to the interrupt queue by the CEI-x30 firmware is indicated by the interrupt queue head pointer, accessed by reading the Interrupt Queue Register. The precise numeric definition for the individual interrupt queue entries is described in the section *Interrupt Queue*, in the chapter CEI-x30 Hardware Interface.

The first type of interrupt event is based on the Receive Label Filter functionality, described in detail in the next section of this chapter. The second type of interrupt event is based on host interaction with the device. Typically used in verification of a custom interrupt service routine, this

type of interrupt is triggered by a host write to the Interrupt Queue Register in the firmware interface. When a write-access to this register is detected, an entry value of 255 is written to the next entry in the interrupt queue and the interrupt queue head pointer value is incremented. You can invoke this feature using the API routine `AR_SET_DEVICE_CONFIG` with the *item* parameter option `ARU_INSERT_INT_Q_ENTRY`.

Hardware interrupts passed on to the PCI bus can be enabled or disabled, independent of the interrupt queue operation. If the `INTERRUPT_ENABLE` bit is set to Enabled in the Global Enable Register, an interrupt is also generated on the PCI bus for each event written to the interrupt queue. You can set this bit by invoking the API routine, `AR_SET_DEVICE_CONFIG`, using the *item* parameter option `ARU_HW_INTERRUPT_ENABLE`.

The CEI-x30 API provides a general interrupt service routine (ISR) for all hardware interrupt processing. When PCI interrupts are enabled, the default ISR logs the interrupt entry in an internal API interrupt buffer, for recall by the API routine, `AR_HW_INTERRUPT_BUFFER_READ`. The host application can replace the invocation of the default ISR with an invocation of a custom host-supplied ISR via the API routine `AR_SET_ISR_FUNCTION`. The host may also defer generation of PCI interrupts and monitor the CEI-x30 device interrupt queue activity via invocation of the API routine `AR_INTERRUPT_QUEUE_READ`.

ARINC 429 Receive Label Filtering and Interrupt Event

The CEI-x30 products provide the capability to both filter received ARINC 429 messages from storage in the circular and snapshot buffers, and generate a PCI interrupt based on matching receive message bit-field values. The trigger definition for ARINC 429 message filtering and interrupt generation is based on the combination of matching 8-bit Label value, 2-bit SDI field value, and 3-bit ESSM field value, with these fields defined within a 32-bit ARINC 429 message as follows:

eSSM	SDI	Label
30, 29, 28	9, 8	7, 6, 5, 4, 3, 2, 1, 0

Each receiver contains a separate label filter table section in which the trigger definition is applied. This table is used by the CEI-x30 firmware to control storage of received labels to both the circular and snapshot buffers and generate a PCI interrupt, with each table entry defined via the CEI-x30 API as follows:

Note:

These definitions are CEI-x20 API-compatible and do not match the actual bit definition defined in the CEI-x30 device Label Filter Table.

<code>FILTER_SEQUENTIAL</code>	0x10	If SET filter label from the circular receive buffer
<code>FILTER_SNAPSHOT</code>	0x20	If SET filter label from the snapshot receive buffer
<code>FILTER_INTERRUPT</code>	0x40	If SET insert channel # in the interrupt queue and if enabled, generate a PCI interrupt

When buffer filtering has been enabled for a specified Label/SDI/ESSM combination, messages received with matching bit field values are discarded for the respective receive buffer until buffer filtering for that specified message has been disabled. Selection of individual and merged circular buffer storage is independent of the filter definition, with the `FILTER_SEQUENTIAL` option being applied to the buffer based on the respective receive channel's active circular buffer storage mode. All label filtering is disabled for each Label/SDI/ESSM combination by default.

When the `FILTER_INTERRUPT` bit is set for a specified label/SDI/ESSM combination, any message received containing that combined field value triggers an entry in the Interrupt Queue. This type of interrupt event is referred to as a *receive interrupt event*, with entry values for receivers 1 through 32 ranging from 64 to 95, respectively.

Transmit Message Processing Methods

The CEI-x30 products provide an individual transmit message buffer mechanization for each installed transmit channel, with two methods of invoking message transmission for the ARINC 429 protocol and a single method of invoking message transmission for the ARINC 573/717 protocol.

Direct access by the host application to individual transmit message buffers is supported for both the ARINC 429 and ARINC 573/717 protocols. Messages are transmitted in the order they are inserted into individual transmit message buffers at the speed at which the respective bus is programmed. General methods supported by the CEI-x30 API for inserting messages into transmit buffers for both protocols include `AR_PUTWORD` for single message insertion, and `AR_PUTBLOCK` and `AR_PUTBLOCK_MULTI_CHAN` for multiple message insertion. Protocol specific methods include `AR_PUT_429_MESSAGE` for single ARINC 429 message insertion and `AR_PUT_573_FRAME` for ARINC 573/717 frame transmission. The individual message format for each of these methods is described in the *Channel Buffer Word 4 - Transmit* section of the CEI-x30 Hardware Interface chapter in this manual.

The CEI-x30 products support an ARINC 429 Message Scheduling feature that allows the host application to offload the requirement to transmit ARINC 429 messages on a periodic basis onto the board. Described in more detail in the next section, this feature provides onboard access to individual transmit message buffers by the firmware-based periodic ARINC 429 message processing. It is important to note the insertion of ARINC 429 messages by the message scheduler into the individual transmit message buffers functions independently from host application message insertion and may result in interwoven message entries when used in conjunction with direct, multiple message insertion API methods.

ARINC 429 Periodic Message Scheduling

The CEI-x30 message scheduling feature supports onboard periodic message transmission of ARINC 429 messages, with 2048 message entries on all actively supported boards. It is programmed by writing message and rate information to the Message Scheduler table, supported by the API routines `AR_DEFINE_MSG`, `AR_DEFINE_MSG_BLOCK`, `AR_MODIFY_MSG`, `AR_MODIFY_MSG_BLOCK` and `AR_ASSIGN_SCHEDULER_START_OFFSETS`. As a part of the API initialization of the device, the Message Scheduler table is reset to an empty state. Once entries are defined by the host application, message scheduling is enabled by invoking the `AR_GO` routine.

When enabled, the Message Scheduler queries each table entry on a one millisecond basis, checking for all messages required for transmission at that particular millisecond value. The entire table is processed each millisecond, with the lowest table entry being processed first and highest table entry last. When invoking `AR_STOP` or `AR_RESET`, it is important to note the scheduler processing responds only to being disabled at the beginning of a one millisecond epoch. If the scheduler is requested to disable in the middle of creating scheduled traffic, all of the ARINC words previously scheduled for that millisecond are loaded into the various transmit buffers before the scheduler transitions to idle.

The efficiency of the Message Scheduler is based on the number of defined messages and the frequency at which those messages are transmitted. While the Message Scheduler feature is designed to be very accurate, there are ways in which the host application definition of channel-specific message transmission scenarios may cause deviations in the periodic transmission of the messages defined therein. The most common deviation is referred to as message rate skew.

Message Rate Skew

Message rate skew is defined as the characteristic of a scheduled message appearing on the bus at a rate that is either above or below the defined periodic rate by a significant percentage. Message rate skew typically occurs when several different message rates are defined simultaneously on the same channel, and a majority of these message rates are multiples of the other message rates. The example below illustrates this situation.

Assuming there are three groups of messages being transmitted at rates of 100 msec (referenced as block A), 200 msec (block B) and 300 msec (block C). If messages from each of the different rate groups were defined in the order of rate priority using same initial starting point of reference, the transmission of data would be defined as follows:

Time	Group
100	A

Time	Group
200	A,B
300	A,C
400	A,B
500	A
600	A,B,C
repeat...	

If we assume that each group of messages requires 10 msec to transmit, we can expand the timeline in more detail as follows:

Time	Group
100	A
200	A
210	B
300	A
310	C
400	A
410	B
500	A
600	A
610	B
620	C
700	A
800	A
810	B
900	A
910	C
etc.	

The time between the first two occurrences of the 300 msec message group (block C) is 310 msec. The time between the second and third occurrences of this group is 290 msec. Message skew like this is unpredictable as the number of different message rates increases.

The solution to this problem is to use the *start offset* feature of the message scheduler, (see the description for AR_DEFINE_MSG). In the next alternative example, the 300 msec message group was defined with a start offset of 20 msec (see note below). In this scenario, no message rate skew would occur, (as shown in the following timeline).

Note:

The 20 msec offset was derived as the sum of the duration required to transmit the groups that precede this group in the scheduling order.

Time	Group
100	A
200	A
210	B
300	A

Time	Group
320	C
400	A
410	B
500	A
600	A
610	B
620	C
700	A
800	A
810	B
900	A
920	C
etc.	

In this transmission example, any start offset from 20 msec to 80 msec would suffice for the 300msec (block C) message group. A start offset greater than 90 msec would cause this message group to overlap into the next scheduled frame for the block A message group and would subsequently induce skewing for those messages.

If the three message rate groups were all even multiples of each other (e.g. 100, 200, and 400 msec) then rate skew would never occur. The good news is that, although the slowest rate messages are most susceptible to rate skew, they are also typically the most tolerant to variation in transmission time.

Since the message scheduler processes all messages in the order of their location in the schedule table, rate skew may also appear on faster rate messages defined further into the table following slower rate messages on the same transmit channel. This type of skew can be easily eliminated on individual transmit channels by defining the faster rate messages for that channel first followed by slower rate messages in descending rate order.

In conclusion, if the minimum rate skew is desired on all transmitted messages, you must make a priority determination of the message loading on each channel and insure messages are scheduled not only with the fastest rates first, but taking full advantage of the start offset feature.

The CEI-x30 API provides a runtime utility routine `AR_ASSIGN_SCHEDULER_START_OFFSETS`, designed to read the current message scheduler channel and label rate content and assign start offsets to each defined message on a best-fit rate-priority basis. This routine should be called after all scheduled messages are defined, prior to activation of message processing on the board.

If you desire manual control of the message transmission scenario, the CEI-x30-SW distribution provides a 32-bit Windows application in the distribution folder \Help\Start Offset Assistant called *gen_offsets.exe*. This application will generate the start offsets for the messages supplied for a set of transmit channels, when supplied in the proper scheduled message data structure input text file format. See the document *Start_Offset_Assistant.pdf* located in the same folder for a description of the application and input file format. Example input and output files are provided to demonstrate the required format.

Avionics Discrete Inputs and Outputs

Most CEI-x30 cards provide individually configurable Avionics Discrete Input/Output channels, used for general avionics-level I/O interfacing. Each discrete output circuit is implemented as a low side FET switch capable of sinking 500mA to ground, while the inputs are single ended, protected (50V max), with a logic threshold of approximately 2.7V. See the paragraph *Avionics Discrete I/O* for a detailed description of the Discrete Input/Output circuit.

To assign a Discrete Output state, use the AR_SET_DEVICE_CONFIG API call with the item parameter selection ARU_DISCRETE_OUT and one of the following value parameter selections:

AR_LO	Discrete Output set to 1 (FET ON – conduct to Ground)
AR_HI	Discrete Output set to 0 (FET OFF – tri-state)

CEI-x30 Hardware Interface

Overview

This chapter describes the low level programming/host interface for all devices available in the CEI-x30 product line.

Note:

The information in this chapter is provided if you intend to author your own software interface and device driver.

Control of a CEI-x30 device is performed by reading and writing the host interface register set, mapped into the host memory space via the BAR0 and/or BAR2 memory regions. PCI and ExpressCard devices use the BAR0 region for PCI target interface configuration registers, and the BAR2 region for all other registers and memory, while native PCI-Express devices do not have a PCI target interface component and use the BAR0 region for all access to registers and memory. To program the PCI and ExpressCard devices, you must first know where these memory regions are mapped in host memory space. In the following sections, the PCI Configuration region and BAR2 (BAR0 for native PCI-Express boards) device configuration registers and buffers are described. All BAR2/BAR0 registers and buffers are 32 bits wide for both read and write access.

The transmit and receive circular buffers are not mapped into the host interface; rather, they are presented as individual buffer entries in the respective channel register set with head/tail pointer management performed by the firmware.

PCI Configuration Space

The following table describes the CEI-x30 PCI Configuration Space definition.

Table 79. CEI-x30 PCI Configuration Space

31	23	15	7	Offset
Device ID NNNNh (0830 for example)		Vendor ID 13C6h		00h
Status		Command		04h
Base class FFh	Sub-class 00h	Interface 00h	Revision ID 00h	08h
BIST Reserved 00h	Header type 00h	Latency Timer Reserved 00h	Cache Line Size Reserved 00h	0Ch
Base Address Register 0 for memory-mapped PCI local configuration registers (or RAR-PCIE FPGA access).				10h
Base Address Register 1 for I/O-mapped PCI local configuration registers.				14h
Base Address Register 2 PCI local bus (FPGA access).				18h
Base Address Register 3 (reserved)				1Ch
Base Address Register 4 (reserved)				20h
Base Address Register 5 (reserved)				24h
Cardbus CIS Pointer (reserved) 00000000h				28h
Subsystem ID NNNNh		Subsystem Vendor ID 13C6h		2Ch
Expansion ROM Base Address (reserved)				30h
Reserved 0x00000000h				34h
Reserved 0x00000000h				38h
MAX_LAT 00h	MIN_GNT 00h	Interrupt pin 00h	Interrupt line	3Ch

PCI Device Identifiers and Resources

The following table provides the PCI Device ID and Subsystem ID values for the CEI-x30 products, along with the BAR memory size allocations for the memory regions utilized with the enhanced firmware configuration:

Table 80. PCI Device ID and BAR Resource Assignments

Product	PCI Device ID	BAR0 (bytes)	BAR1 (bytes)	BAR2 (bytes)
CEI-430	0430h	128	0	512K
RCEI-430A	430Ah	128	0	512K
CEI-830	0830h	512	256	512K
R830RX	0831h	512	256	512K
RCEI-530	0530h	512	256	512K
RAR-CPCI	0630h	512	256	512K
RAR-EC	100Ah	128	0	512K
RAR-PCIE	100Bh	512K	0	0
RAR-XMC	100Ch	512K	0	0
AMC-A30	1009h	512	256	512K
RCEI-830X820	0832h	512	256	512K
RCEI-830A	830Ah	512	256	512K
RAR-MPCIE	100Dh	512K	0	0

Host Memory Map

The following table summarizes the memory-mapped host interface for the CEI-x30 device firmware, described in detail in the following sections.

Table 81. CEI-x30 Host Memory Map

Byte Address	Read/Write	Device Interface Register Description
0x00000	Read/Write	Global Enable Register
0x00004	Write only	DAC Control Register
0x00008	Read/Write	Timer Register (least significant 32 bits)
0x0000C	Read/Write	Timer Register (most significant 32 bits)
0x00010	Write only	Update IRIG Generator Time Register
0x00014	Read only	IRIG Sample Time Register
0x00018	Read only	IRIG Sample Timestamp Register (least significant 32 bits)
0x0001C	Read only	IRIG Sample Timestamp Register (most significant 32 bits)
0x00020	Write only	SRAM Address Register
0x00024	Read/Write	SRAM Data Register
0x00028 – 0x0037	Read only	General Input Registers 1-4
0x00038	Read/Write	Interrupt Queue Register
0x0003C		Unused
0x00040 – 0x0005F		MIL-STD-1553 Channel Timers (RAR15-XMC only)
0x00040	Read only	Channel 1 timer - least significant 32 bits
0x00044	Read only	Channel 1 timer - most significant 32 bits
0x00048	Read only	Channel 2 timer - least significant 32 bits
0x0004C	Read only	Channel 2 timer - most significant 32 bits
0x00050	Read only	Channel 3 timer - least significant 32 bits
0x00054	Read only	Channel 3 timer - most significant 32 bits
0x00058	Read only	Channel 4 timer - least significant 32 bits
0x0005C	Read only	Channel 4 timer - most significant 32 bits
0x00060	Read/Write	ARINC 429 Rx BIT Command (RAR15-XMC only)
0x00064	Read only	ARINC 429 Rx BIT Response Word 1 (RAR15-XMC only)
0x00068	Read only	ARINC 429 Rx BIT Response Word 2 (RAR15-XMC only)
0x0006C – 0x0007F		Unused
0x00080	Read only	Board temperature (RAR-PCIE, RAR-MPCIE, RAR-XMC and CEI-430A only)
0x00084	Read only	Voltage Monitor +1.0V (RAR-PCIE only)
0x00088	Read only	Voltage Monitor +2.5V (RAR-PCIE only)
0x0008C – 0x003FF		Unused
0x00400 – 0x007FF	Read only	Channel Statistics Table
0x00800 – 0x03FFF		Unused
0x04000 – 0x07FFF		Channel Register Set
0x00	Read only	Channel Status Register
0x04	Read/Write	Channel Configuration Register 1

Byte Address	Read/Write	Device Interface Register Description
0x08	Read/Write	Channel Configuration Register 2 (ARINC 717 Only)
0x0C	Read/Write	Channel Configuration Register 3 (ARINC 717 Only)
0x10	Read only	Channel Buffer Word 1 (Receive only)
0x14	Read only	Channel Buffer Word 2 (Receive only)
0x18	Read only	Channel Buffer Word 3 (Receive only)
0x1C	Read or Write	Channel Buffer Word 4 (Read for Receive, Write for Transmit)
0x20 – 0x3F		Spare
0x08000 – 0x09FFF	Read Only	Interrupt Queue
0x0A000 – 0x1FFFF		Unused
0x20000 – 0x2FFFF	Read/Write	Message Scheduler Table (0x27FFF for CEI-830)
0x28000 – 0x3FFFF		Unused
0x40000 – 0x7FFFF	Read Only	Snapshot Buffer

Device Interface Register Set (Common Memory)

Global Enable Register

31	30	29 – 24	23 - 16	15 - 8	7	6	5	4	3	2	1	0
Device Disable / Auton Set	Auton Clear	Not Used	F/W Vers.	Board Config	IRIG Output Enable	Snapshot Mode	Interrupt Enable	Interrupt Pending	IRIG Edge Detect	IRIG Present	IRIG Internal Wrap	Global Enable

The fields in the Global Enable register are described as follows:

Field	Description	Values
GLOBAL ENABLE	This bit is used to enable and disable transmit and receive operation of the device. When disabled, data transfer between the transmit and receive FIFOs in SRAM are cleared. Individual channel data (de)serialization processes is disabled. This bit also enables and disables message scheduler operation.	0 = disabled (reset condition) 1 = enabled
IRIG INTERNAL WRAP	This bit is used to enable and disable internal connection of the on-board IRIG generator to the IRIG receiver.	0 = wrap disabled 1 = wrap enabled
IRIG PRESENT (read only)	This bit indicates whether or not IRIG hardware is installed.	0 = IRIG not installed 1 = IRIG installed
IRIG EDGE DETECT (read only)	This bit indicates an IRIG signal edge was detected on the IRIG receiver input pins. This bit is cleared when this register is read. This bit is used to help determine the appropriate IRIG receive threshold level.	0 = IRIG edge not detected 1 = IRIG edge detected
INTERRUPT PENDING	When this bit is set, a PCI interrupt is pending. Writing the Global Enable Register with this bit set clears the pending interrupt in the firmware interface.	0 = undefined 1 = (read) interrupt pending (write) clear pending interrupt
INTERRUPT ENABLE	This bit enables generation of PCI interrupts from the label filter table trigger mechanism.	0 = PCI interrupt disabled 1 = PCI interrupt enabled
SNAPSHOT MODE	This bit defines how received ARINC 429 messages are stored in the snapshot buffer.	0 = storage using label + SDI 1 = storage using label only
IRIG OUTPUT ENABLE (R830RX only)	This bit enables IRIG Generator signal output on P1 pins 33 and 66, P14 pins 63 and 64, when jumper shunt sets J4 and J5 are shorted	0 = IRIG Output disabled 1 = IRIG Output enabled

Field	Description	Values
BOARD CONFIGURATION (read only)	This bit field indicates the programmed configuration of the device.	7 = CEI-830 8 = CEI-430 9 = AMC-A30 10 = CEI-530 11 = R830RX 12 = RAR-CPCI 13 = RAR-EC 14 = RAR-PCIE 15 = CEI-430A 16 = N/A 17 = (R)AR15-XMC 18 = RCEI-830X820 19 = RAR-XMC 20 = RCEI-830A 21 = RAR-MPCIE
FIRMWARE VERSION (read only)	This bit field indicates the version of firmware programmed on the board. Added in firmware v4.08.	2-digit value, 4 bits/digit
AUTON CLEAR (write only)	This Autonomous Clear bit is required to be set when clearing any bit field in the Global Enable Register	0 = no operation on write access 1 = bitwise clear of any writeable bit for any bit set from b0 to b7
DEVICE DISABLE (read only)	This bit indicates the on-board security feature has disabled the board. This bit is not supported by the CEI-830.	0 = device enabled 1 = device disabled
AUTON SET (write only)	This Autonomous Set bit is required to be set when setting any writable bit field in the Global Enable Register	0 = no operation on write access 1 = bitwise set of any writeable bit for any bit set from b0 to b7

DAC Control Register

The DAC Control Register determines the IRIG Receiver voltage threshold and the AMC-A30 Discrete Input voltage threshold. The optimal threshold for a DC level IRIG signal is the midpoint between the upper and lower voltage levels of the IRIG signal. An appropriate level for an AM encoded IRIG signal is at the 80% point between the upper and lower voltage levels of the IRIG signal. The 80% value is acceptable for a DC signal, and should be used if the host does not know which encoding (DC or AM) is used.

For the AMC-A30, the Discrete Input voltage threshold is set when bit 8 of the DAC control register is set high, otherwise, the IRIG Receiver voltage threshold will be selected. The default Discrete Input voltage threshold level is 10.2 volts.

31 - 9	8	7 - 0
N/A	AMC-A30 DAC Select	DAC Value IRIG DAC value = $(128 + ((256/3.3) * (4.99/22.1) * V_{IRIG_Threshold}))$ Where $V_{IRIG_Threshold}$ is the value in Volts for the IRIG receive threshold relative to the input pins. Discrete DAC value = $0.3V + (256/3.3) * V_{Discrete_In_Threshold}$
	0 = IRIG 1 = Discrete	

Timer Registers

These two registers contain the current 64-bit 1μsec device timer value. When reading these registers, the Time-Tag High Word is latched when the Time-Tag Low Word is read. When writing these registers, the value written to the Time-Tag Low Word is latched and stored and the entire 64-bit timer is updated when the Time-Tag High Word is written. For this reason, the Time-Tag Low Word must always be read or written before the Time-Tag High Word or the combined contents will be invalid.

31 - 0
Time-Tag Low Word

The least significant 32-bits of the 64-bit timer, 1μsec resolution.

31 - 0
Time-Tag High Word

The most significant 32-bits of the 64-bit timer, resolution is approximately 71.58 minutes.

Multi-protocol Timer Registers

These 8 registers contain the current MIL-STD-1553 timer values, and they are latched when the Time-Tag Low Word is read. These registers are used to correlate MIL-STD-1553 timestamps with ARINC timestamps. The resolution of the MIL-STD-1553 timers is one nanosecond. See the MIL-STD-1553 UCA API manual for information on programming the MIL-STD-1553 timers. These registers are only supported on multiple-protocol RAR15-XMC boards.

31 - 0
MIL-STD-1553 CH1 Timer Low Word

31 – 0
MIL-STD-1553 CH1 Timer High Word

31 – 0
MIL-STD-1553 CH2 Timer Low Word

31 – 0
MIL-STD-1553 CH2 Timer High Word

31 – 0
MIL-STD-1553 CH3 Timer Low Word

31 – 0
MIL-STD-1553 CH3 Timer High Word

31 – 0
MIL-STD-1553 CH4 Timer Low Word

31 – 0
MIL-STD-1553 CH4 Timer High Word

Update IRIG Generator Time Register

This register provides the means to assign the current IRIG time-of-year for the IRIG generator circuit. The format follows the standard IRIG 30-bit encoded time-of-year. The upper two bits of this register are unused. This register is only valid if the Global Enable “IRIG Installed” bit is set.

29-28	27-24	23-20	19-18	17-14	13-11	10-7	6-4	3-0
hundreds of days	tens of days	days	tens of hours	hours	tens of minutes	minutes	tens of seconds	seconds

IRIG Sample Time Register

This register contains the last received IRIG bit-encoded time value. This register is only valid if the Global Enable “IRIG Installed” bit is set.

29-28	27-24	23-20	19-18	17-14	13-11	10-7	6-4	3-0
hundreds of days	tens of days	days	tens of hours	hours	tens of minutes	minutes	tens of seconds	seconds

IRIG Sample Timestamp Registers

These two registers contain the device-referenced timer timestamp recorded when the last IRIG time one-second sample was received. The device will read the current 64-bit 1μsec device timer value when the first bit of the IRIG time is detected and store it in these registers when the IRIG Sample Time Register is updated. When reading these registers the Time-Tag High Word is latched when the Time-Tag Low Word is read. For this reason, the Time-Tag Low Word must always be read before the Time-Tag High Word or the combined contents will be invalid.

31 – 0
Time-Tag Low Word

The least significant 32-bits of the 64-bit time-tag, resolution is 1μsec.

31 – 0
Time-Tag High Word

The most significant 32-bits of the 64-bit time-tag, resolution is approximately 71.58 minutes.

SRAM Access Address Register

This register provides a means to access the CEI-x30 on-board SRAM through the FPGA interface. The value assigned to this register is an offset into the SRAM memory device, from 0 to 0x7FFFF, selecting the SRAM address at which a read or write access will occur based on a subsequent operation with the SRAM Access Data Register.

SRAM Access Data Register

This register defines the type of operation to perform on the SRAM location specified in the SRAM Access Address Register. A read from this register will result in a read and return the current 32-bit value in that SRAM location, where a write to this register will result in a write of the 32-bit value to the respective SRAM location. Writes to this register should be done carefully, since every SRAM location, including locations used for label filtering tables, receive and transmit buffering, and other internal functions, can be altered by this mechanism.

General Input Registers

General Input Register 1 - Discrete Inputs

For each Discrete Input on the device, a single bit is allocated in General Input Register 1. The Discrete Input bit assignments start with the LSB, b0 as Discrete Input 1, b1 as Discrete Input 2, and increment by Discrete Input Channel value through b31. Unpopulated inputs are always zero.

General Input Register 2 - Differential Inputs

For each Differential Input on the CEI-430, a single bit is allocated in General Input Register 2. The Differential Input bit assignments are b0 for Differential Input 1, b1 for Differential Input 2, b2 for Differential Input 3, and b3 for Differential Input 4. Unpopulated inputs are always zero.

General Input Registers 3 and 4 are currently unused.

Interrupt Queue Register

The Interrupt Queue Register has different definitions based on the access method used. When written, the Interrupt Queue Register is used to generate a single host-defined entry in the Interrupt Queue, having a value of 255. When read, the Interrupt Queue Register provides the current Interrupt Queue Head Pointer, pointing to the most recent interrupt entry in the queue and defined as follows:

31 – 11	10 – 0
Unused	Current offset into the Interrupt Queue for the most recent entry, with a valid range of 0 – 2047.

ARINC 429 Receiver BIT Function

The RAR15XF and RAR15-XMC-IT products provide an on-board ARINC 429 Receiver BIT Function that validates the signal path to the Receiver circuit. Invocation of the BIT function is controlled by the Receiver BIT Command register and verified via the differential input bit field values in the Receiver BIT Response Words.

Receiver BIT Command

The Receiver BIT Command register is defined as follows:

31 – 2	1 – 0
Unused	Receiver BIT Command values: 0 – Receiver BIT Response bit values reflect the current state of the input pin 1 – Set the differential A input to 0, B input to 1 2 – Set the differential A input to 1, B input to 0 3 – Set the differential A input to 0, B input to 0

Receiver BIT Response Words

The Receiver BIT Response Words contain the current input states for the A and B differential pair receiver circuits, encoded in a 2-bit field for each receiver installed on the board. For configurations with fewer receivers than what is shown below, the respective bit field should be considered Reserved.

The Receiver BIT Response Word 1 register contains the A and B differential pair input states for Receivers 1 through 10 (if installed), encoded as follows:

31-20	19-18	17-16	15-14	13-12	11-10	9-8	7-6	5-4	3-2	1-0
Reserved	Rx 10 A/B	Rx 9 A/B	Rx 8 A/B	Rx 7 A/B	Rx 6 A/B	Rx 5 A/B	Rx 4 A/B	Rx 3 A/B	Rx 2 A/B	Rx 1 A/B

The Receiver BIT Response Word 2 register contains the A and B differential pair input states for Receivers 11 through 18 (if installed), encoded as follows:

31-16	15-14	13-12	11-10	9-8	7-6	5-4	3-2	1-0
Reserved	Rx 18 A/B	Rx 17 A/B	Rx 16 A/B	Rx 15 A/B	Rx 14 A/B	Rx 13 A/B	Rx 12 A/B	Rx 11 A/B

Channel Statistics Table

The Channel Statistics Table contains one entry for each of the 256 channels allocated on the device. Each entry contains a 32-bit counter whose definition is based on whether the channel is a receive or transmit channel. For a receive channel, the respective entry indicates the number of messages received on that channel since the board was last initialized. For a transmit channel, the respective entry indicates the number of messages transmitted on that channel since the board was last initialized.

Channel Register Set

The Channel Register Set contains the status, configuration, and buffer access registers for all 256 channels allocated on the device. Each channel register sub-set is defined as shown below with the respective offset:

Channel Status Register	0x0000
Channel Configuration Register 1	0x0004
Channel Configuration Register 2	0x0008
Channel Configuration Register 3	0x000C
Channel Buffer Word 1	0x0010
Channel Buffer Word 2	0x0014
Channel Buffer Word 3	0x0018
Channel Buffer Word 4	0x001C

These components of the Channel Register Set are defined in the next several paragraphs of this chapter.

Channel Status Register

The Channel Status Register has a common bit field definition across all channels, but other than the Channel Type bit field, its use only applies to those channels defined for protocol processing. The Channel Status Register is defined as follows:

31 - 16	15	14 - 8	7 - 3	2	1	0
Buffer Fill Level	Channel Inactive	Channel Type	Unused	Buffer Overflow	Message Error	Buffer Status

The fields in the Channel Status Register are described as follows:

Field	Description	Values
BUFFER FILL LEVEL (read only)	For a receive channel, this field indicates the number of unread messages currently in the receive buffer. For a transmit channel, this field indicates the number of "untransmitted" messages residing in the transmit buffer.	0 to 2047
CHANNEL INACTIVE (read only)	This field indicates this channel is inactive for this board configuration (for shared pin-out usage with optional component configurations)	0 = channel active for ARINC protocol usage 1 = channel inactive for ARINC protocol usage
CHANNEL TYPE (read only)	This field indicates the channel type assigned to this Channel Register Set.	0 = unassigned channel 1 = Merged Mode Receiver 2 = ARINC 429 Receiver 3 = ARINC 429 Transmitter 4 = ARINC 717 Receiver 5 = ARINC 717 Transmitter 6 = ARINC 561 Receiver 7 = ARINC 561 Transmitter 8 = Avionics Discrete Input 9 = Avionics Discrete Output 10 = Digital Input 11 = Digital Output 12 = Differential Input 13 = Differential Output 14 = Serial Receiver 15 = Serial Transmitter 16 = Shared ARINC 429 Receiver 17 = Shared ARINC 429 Transmitter 16 to 255 = Undefined
BUFFER OVERFLOW (read/write)	This bit is set to "1" when an ARINC 429 buffer overflow condition is detected on the respective receive channel. This bit is cleared when a "1" is written to it by the host.	0 = normal buffer condition 1 = a buffer overflow condition was detected since this bit was last cleared
MESSAGE ERROR (read/write)	This bit is set to "1" when an ARINC 429 message length error is detected on the respective receive channel. This bit is cleared when a "1" is written to it by the host.	0 = no message error detected 1 = a message bit length error was detected since this bit was last cleared
BUFFER STATUS (read only)	For a receive channel, the Buffer Status bit indicates the availability of unread messages. For a transmit channel, the Buffer Status bit indicates the fill-state of the buffer.	Receive Channel: 0 = no messages in the buffer 1 = an unread message is available in the buffer Transmit Channel: 0 = buffer is not full 1 = buffer is full

Channel Configuration Registers

The definition of the Channel Configuration Registers is dependent on the associated channel type, and their use only applies to those channels defined for protocol processing. The specific Channel Configuration Register types are described in the following paragraphs, categorized by channel type, as well as receive and transmit usage.

Input Channel Config Register 1 – ARINC 429 Receive

When Channel Configuration Register 1 is allocated as an Input Channel Configuration Register for ARINC 429 protocol reception, it is defined as follows:

31-28	27 - 16	15	14	13-10	9	8 - 3	2	1	0
Not Used	Baud Rate	Channel Enable	Merge Mode Enable	Not Used	Message Length	Not Used	Internal Wrap Enable	Parity Enable	Not Used

The bit fields in the ARINC 429 Receive Channel Configuration Register are described as follows:

Field	Description	Values
PARITY ENABLE	This bit is used to enable and disable parity checking on the received ARINC 429 data.	0 = disabled (reset condition) 1 = enabled
INTERNAL WRAP ENABLE	This bit is used to enable and disable the ability to wrap transmitted data internal to the device. Each receive channel is internally connected to the respective transmitter channel.	0 = disabled (reset condition) 1 = enabled
MESSAGE LENGTH	This bit defines the expected message length to be either 32 bits or 24 bits.	0 = 32 bits 1 = 24 bits
MERGE MODE ENABLE	This bit controls the path for storage of received data on the respective channel. When disabled, all received data is stored in the individual receive FIFO for the respective channel. When enabled, all received data is stored in the merged receive FIFO, accessed via channel 0.	0 = disabled (reset condition) 1 = enabled

Field	Description	Values
CHANNEL ENABLE ¹	This bit controls the receiver's conversion of incoming ARINC 429 data for transfer to the respective FIFO buffer. Any transition from disabled to enabled will flush the respective receive buffer.	0 = disabled (reset condition) 1 = enabled
BAUD RATE	This bit field controls the baud rate for the ARINC 429 protocol. The value of this field is used as a divisor for the 20MHz or 16MHz clock reference.	For the RAR15-XMC and RAR15-XMC-XT boards: Baud Rate = 20,000,000/(N+2) Otherwise it is: Baud Rate = 16,000,000/(N+2)

Input Channel Config Register 1 – ARINC 717 Receive

When Channel Configuration Register 1 is allocated as an Input Channel Configuration Register for ARINC 717 protocol reception, it is defined as follows:

31-16	15	14	13	12	11 - 8	7-3	2	1-0
Not Used	Channel Enable	Merge Mode Enable	ARINC 717 Raw Mode Enable	ARINC 717 Encoding	ARINC 717 Rate & Size	Not Used	Internal Wrap Enable	Not Used

The bit fields in the ARINC 717 Receive Channel Configuration Register are described as follows:

Field	Description	Values
INTERNAL WRAP ENABLE	This bit is used to enable and disable the ability to wrap transmitted data internal to the device. Each receive channel is internally connected to the respective transmitter channel.	0 = disabled (reset condition) 1 = enabled

¹ When ARINC 429 Receive CHANNEL ENABLE is disabled, no message reception operations are performed. When enabled, the respective receive buffer will be flushed of all existing messages and messages subsequently received will be processed for storage in the buffer.

Field	Description	Values																											
ARINC 717 RATE & SIZE	This bit field selects the ARINC 717 baud rate and respective sub-frame size for use when Auto-Sync reception is enabled.	<table> <tr> <th>Value</th><th>Speed (bps)</th><th>Sub-frame Size (words)</th></tr> <tr><td>0x00</td><td>384</td><td>32</td></tr> <tr><td>0x01</td><td>768</td><td>64</td></tr> <tr><td>0x02</td><td>1536</td><td>128</td></tr> <tr><td>0x03</td><td>3072</td><td>256</td></tr> <tr><td>0x04</td><td>6144</td><td>512</td></tr> <tr><td>0x05</td><td>12288</td><td>1024</td></tr> <tr><td>0x06</td><td>24576</td><td>2048</td></tr> <tr><td>0x07</td><td>49152</td><td>4096</td></tr> </table>	Value	Speed (bps)	Sub-frame Size (words)	0x00	384	32	0x01	768	64	0x02	1536	128	0x03	3072	256	0x04	6144	512	0x05	12288	1024	0x06	24576	2048	0x07	49152	4096
Value	Speed (bps)	Sub-frame Size (words)																											
0x00	384	32																											
0x01	768	64																											
0x02	1536	128																											
0x03	3072	256																											
0x04	6144	512																											
0x05	12288	1024																											
0x06	24576	2048																											
0x07	49152	4096																											
ARINC 717 ENCODING	This bit selects the ARINC 717 encoding supported by the receiver. When internal wrap is enabled, the value of this bit has no effect on data reception.	0 = Harvard Bi-Phase (HBP) 1 = Bi-Polar Return-to-Zero (BPRZ)																											
ARINC 717 RAW MODE ENABLE	This bit disables the receiver automatic frame detection logic on the incoming ARINC 717 frame data and enables "Raw Mode". When disabled, the receiver will automatically synchronize to the incoming frame using the sub-frame size selection and the sync words programmed in the configuration words 1 through 4 for the respective channel. When Raw Mode is enabled, frame data will be logged to the receive buffer beginning with the first bit encountered from the ARINC 717 receiver.	0 = disabled (reset condition) 1 = Raw Mode enabled																											
MERGE MODE ENABLE	This bit controls the path for storage of received data on the respective channel. When disabled, all received data is stored in the individual receive FIFO for the respective channel. When enabled, all received data is stored in the merged receive FIFO, accessed via channel 0.	0 = disabled (reset condition) 1 = enabled																											
CHANNEL ENABLE	This bit controls the receiver's conversion of incoming ARINC 717 data for transfer to the respective FIFO buffer. When disabled, no data reception operations are performed. When enabled, data reception operations are performed, and data is processed for storage in the receiver's FIFO buffer.	0 = disabled (reset condition) 1 = enabled																											

Input Channel Config Register 2 – ARINC 717 Receive

31 - 28	27 - 16	15 - 12	11 - 0
Not used	Sync Word 2	Not used	Sync Word 1

Input Channel Config Register 3 – ARINC 717 Receive

31 - 28	27 - 16	15 - 12	11 - 0
Not used	Sync Word 4	Not used	Sync Word 3

When the Channel Register Set is assigned to an ARINC 717 Receive Channel, Input Channel Configuration Registers 2 and 3 specify the respective ARINC 717 sub-frame sync words 1-4. These registers support definition of the four 12-bit sub-frame sync words and are only used when ARINC 717 Auto Sync is enabled. All four fields must be defined for the Auto Sync feature to function.

Output Channel Config Register 1 – ARINC 429 Transmit

When Channel Configuration Register 1 is allocated as an Output Channel Configuration Register for ARINC 429 protocol transmission, it is defined as follows:

31-28	27 - 16	15	14 - 10	9	8	7	6	5	4	3	2	1	0
Not Used	Baud Rate	Channel Enable	Unused	Message Length	Not Used	Parametric Mode	Transmit Disable	Gap Error	Bit Count High	Bit Count Low	Even Parity	Parity Enable	Slew Rate

The bit fields in the ARINC 429 Transmit Channel Configuration Register are described as follows:

Field	Description	Values
SLEW RATE	This bit is used to select the slew rate utilized with the ARINC 429 protocol.	0 = Slow Slew Rate (10 μ sec) 1 = Fast Slew Rate (1.5 μ sec)
PARITY ENABLE	This bit is used to enable and disable parity application to the transmitted ARINC 429 message.	0 = disabled (reset condition) 1 = enabled

Field	Description	Values
EVEN PARITY	This bit is used to select between even and odd parity when ARINC 429 message parity is under device control. When enabled, even parity is applied, when disabled, odd parity is applied.	0 = odd parity (reset condition) 1 = even parity
BIT COUNT LOW ¹	This bit is used to enable a low bit count error for ARINC 429 messages, resulting in the transmission of 31 bits instead of 32.	0 = disabled (reset condition) 1 = enabled
BIT COUNT HIGH ¹	This bit is used to enable a high bit count error for ARINC 429 messages, resulting in the transmission of 33 bits instead of 32.	0 = disabled (reset condition) 1 = enabled
GAP ERROR ¹	This bit is used to induce a message gap error between ARINC 429 message transmissions, resulting in a two-bit gap instead of the standard four-bit gap.	0 = disabled (reset condition) 1 = enabled
TRANSMIT DISABLE	This bit is used to disable external transmission to the respective ARINC 429 transmitter. This provides for the ability to transmit internally to the respective receiver with internal wrap enabled, without exposing the communications to a connected device. For products that have the ability to tri-state the transmit output, setting this bit will cause the output to be tri-stated. For all other products, setting this bit will cause the output to remain a "null".	0 = disabled (reset condition) 1 = enabled
MESSAGE LENGTH	This bit defines the transmitted message length to be either 32 bits or 24 bits.	0 = 32 bits 1 = 24 bits
PARAMETRIC MODE	This bit is used to enable parametric operation on the respective transmit channel DAC.	0 = disabled (reset condition) 1 = enabled
CHANNEL ENABLE	For ARINC 429 transmitters, this bit controls the conversion of data passed from the transmitter FIFO for transmission on the bus. When disabled, no data transmission operations are performed. When enabled, data transmission operations are performed using data provided from the specified transmitter's FIFO buffer.	0 = disabled (reset condition) 1 = enabled

¹ This function is only supported by channels with a CHANNEL TYPE indicating *ARINC 429 Transmitter* with PARAMETRIC MODE enabled.

Field	Description	Values
BAUD RATE	This bit field controls the baud rate for the ARINC 429 protocol. The value of this field is used as a divisor for the 20MHz or 16MHz clock reference.	For the RAR15-XMC and RAR15-XMC-XT boards: Baud Rate = 20,000,000/(N+2) Otherwise it is: Baud Rate = 16,000,000/(N+2)

Output Channel Config Register 1 – ARINC 717 Transmit

When Channel Configuration Register 1 is allocated as an Output Channel Configuration Register for ARINC 717 protocol transmission, it is defined as follows:

31-16	15	14	13	12	11 - 8	7	6	5-0
Not Used	Channel Enable	Unused	ARINC 717 HBP Encoding	ARINC 717 BPRZ Encoding	ARINC 717 Baud Rate	Not used	Transmit Disable	Not used

The bit fields in the ARINC 717 Transmit Channel Configuration Register are described as follows:

Field	Description	Values
TRANSMIT DISABLE	This bit is used to disable external transmission to the respective ARINC 573 transmitter (either HBP or BPRZ). This provides for the ability to transmit internally to the respective receiver with internal wrap enabled, without exposing the communications to a connected device. For products that have the ability to tri-state the transmit output, setting this bit will cause the output to be tri-stated. For all other products, setting this bit will cause the output to remain a "null".	0 = disabled (reset condition) 1 = enabled
ARINC 717 BAUD RATE	This bit field selects the ARINC 717 baud rate.	0 = 384 bps 1 = 768 bps 2 = 1536 bps 3 = 3072 bps 4 = 6144 bps 5 = 12288 bps 6 = 24576 bps 7 = 49152 bps
ARINC 717 BPRZ ENCODING	This bit enables the ARINC 717 Bi-Polar Return-to-Zero (BPRZ) encoding transmitter.	0 = disabled (reset condition) 1 = enabled

Field	Description	Values
ARINC 717 HBP ENCODING	This bit enables the ARINC 717 Harvard Bi-Phase (HBP) encoding transmitter.	0 = disabled (reset condition) 1 = enabled
CHANNEL ENABLE	For ARINC 717 transmitters, this bit controls the conversion of data passed from the transmitter FIFO for transmission on the bus. When disabled, no data transmission operations are performed. When enabled, data transmission operations are performed using data provided from the specified transmitter's FIFO buffer.	0 = disabled (reset condition) 1 = enabled

Output Channel Config Register 1 – Discrete or Digital Output

When Channel Configuration Register 1 is allocated as an Output Channel Configuration Register for Discrete or Digital Output, it is defined as shown below. The definition of the Discrete Output State is discussed in the section, “Avionics Discrete I/O”.

31 – 1	0
Unused	Discrete Output State

Output Channel Config Register 1 – Differential Output

When Channel Configuration Register 1 is allocated as an Output Channel Configuration Register for Differential Output, it is defined as shown below. The definition of the Differential Output State is discussed in the section, “Differential Discrete I/O”.

31 – 2	1	0
Unused	Differential Output Enable 0 = tri-state 1 = enabled	Differential Output State

Channel Buffer Words

The definition of the Channel Buffer Words is dependent on the associated channel type. Use of the different Channel Buffer Word sets is described in the following paragraphs, categorized by receive, transmit, and I/O usage.

General Buffer FIFO Operations

Protocol-based Input and Output (Receive and Transmit) Channel Configuration Register Sets control the processing related to the corresponding FIFO buffer for message storage, accessed via Channel Buffer Words. FIFO buffer access is completely independent of either of the Global Enable or Individual Channel Enable states, with host access to FIFO buffers and firmware head/tail processing enabled immediately following initialization of the board. Regardless of the state of the “enable” bits, the host can read available data from and write data to, any applicable FIFO buffer.

Channel Buffer Word 1 - Receive

31 – 0
Time-Tag Low Word

When the Channel Status Register indicates a receiver FIFO is not empty, Channel Buffer Word 1 contains the least significant 32 bits of the 64-bit time-tag. The resolution of this time-tag low word is 1μsec.

Channel Buffer Word 2 - Receive

31 – 0
Time-Tag High Word

When the Channel Status Register indicates the FIFO is not empty, Channel Buffer Word 2 contains the most significant 32 bits of the 64-bit time-tag. The resolution of this time-tag high word is approximately 71.58 minutes.

Channel Buffer Word 3 – Receive

31 – 8	7 – 0
Not used (all zeros)	Channel

When the Channel Status Register indicates the FIFO is not empty, Channel Buffer Word 3 contains the channel on which this data was received. This information is useful when the Merged Mode channel is enabled and utilized for the respective receive channel.

Channel Buffer Word 4 – Receive

31 – 0
Data

When the Channel Status Register indicates the FIFO is not empty, Channel Buffer Word 4 contains the data that was received.

Note:

When the host reads Channel Buffer Word 4, the receiver FIFO for the selected channel is incremented to the next entry. This could result in a FIFO Not Empty reset in the respective Receive Status register if the FIFO becomes empty. This implies Channel Buffer Word 4 should be the last register accessed when reading a complete FIFO buffer entry. It is NOT necessary to read all four Receive Buffer Word registers from the FIFO if the respective information is not needed.

The format for the data retrieved from Receive Buffer Word 4 is dependent on the protocol assigned to the respective channel. The protocol data format is described as follows:

ARINC 429/575 32-bit Data Format

31	30 – 10	9 - 8	7 - 0
Parity Indication or ARINC Data MSB	ARINC Data	SDI bits or ARINC Data bits 0-1	ARINC Label (MSB – LSB)

ARINC 585 24-bit Data Format

31 - 24	23	22 - 0
Unused	Parity Indication or ARINC Data MSB	ARINC Data

If the Parity Enable bit is set to one in the respective Receive Configuration register, the Parity Indication is set by the device to indicate the parity of the message. A Parity Indication bit value of zero indicates this message was received with odd parity, where a Parity Indication value of one indicates the message was received with even parity. If the Receive Configuration Register Parity Enable bit is set to zero, this bit is not manipulated by the device; instead, it reflects the value of the message MSB as transmitted from the ARINC 429/585 source.

ARINC 717 Data Format

31 – 16	15	14	13 - 12	11 – 0
Unused	Sync Indication	Unused	Sub-frame Identification	Data Word

When the Sync Indication bit is set to one, it is an indication this word was detected as a sync word. A Sync Indication bit value of zero indicates the message was treated as a data word. The Sub-frame Identification bit field identifies the sub-frame assignment for this word; where a value of one indicates sub-frame 1, two indicates sub-frame 2, three indicates sub-frame 3, and zero indicates sub-frame 4.

Channel Buffer Words 1, 2, and 3 - Transmit

Channel Buffer Words 1, 2, and 3 are not currently used for Transmit.

Channel Buffer Word 4 - Transmit

31 – 0
Data

When the Channel Status Register indicates the FIFO is not full, Channel Buffer Word 4 can be defined for transmission on the respective channel.

Note:

When the host writes the most significant byte of Channel Buffer Word 4, the transmitter FIFO for the selected channel is incremented to the next entry. This could result in a FIFO Not Full reset in the respective Transmit Status register if the FIFO becomes full.

The format for the data written to Channel Buffer Word 4 is dependent on the protocol assigned to the respective channel. The protocol data format is described as follows:

ARINC 429/575 Data Format

31	30 – 10	9 – 8	7 – 0
Parity Bit or ARINC Data MSB	ARINC Data	SDI bits or ARINC Data bits 0-1	ARINC Label (MSB – LSB)

ARINC 585 24-bit Data Format

31 - 24	23	22 - 0
Unused	Parity Bit or ARINC Data MSB	ARINC Data

If the Parity Enable bit is set to *Enabled* in the respective Transmit Configuration register, the Parity Bit (MSB) of the ARINC data word will be overwritten by the device. The value assigned to the Parity Bit is based on the parity type and bit content of the remaining data bits. If the Transmit Register Parity Enable bit is set to zero (transmit parity disabled), the Parity Bit remains unchanged from the value provided.

ARINC 717 Data Format

31 – 12	11 – 0
Unused	Data Word

ARINC 717 data is assigned to the lower 12 bits of the 32-bit word.

Interrupt Queue

The CEI-x30 Interrupt Queue contains 2048 32-bit entries, each indicating the source of an interrupt trigger. The most recent Interrupt Queue entry updated by the CEI-x30 device is indicated via the Interrupt Queue Head Pointer, accessed by reading the Interrupt Queue Register.

Valid Interrupt Queue entries are defined as follows:

31 – 8	7 - 0
Unused	Interrupt Queue Entry Definition: Values in the ranges 0–63 and 128–254 are unused 64–127 = Interrupt Source/Receive Channel Number 0 to 63, (offset by 64) 255 = Host generated interrupt via write access to the Interrupt Queue Register.

Message Scheduler Table

The CEI-x30 Message Scheduler feature is programmed via the Message Scheduler Table, a table of 2048 entries, each consisting of eight 32-bit elements (1024 entries only for the CEI-830). As a part of the initialization of the device, the message scheduler table should be initialized to a known state. This is required before the message scheduler is enabled; otherwise, inadvertent message transmission may result. The GLOBAL ENABLE bit of the Global Enable Register turns message scheduling on and off; however, it has no effect on the contents of the message schedule table.

The Message Scheduler will query each table entry on a one millisecond basis, checking for all messages required for transmission at that particular millisecond value. The entire table is processed each millisecond, with the lowest table entry being processed first and highest table entry last. The scheduler can only be enabled or disabled at the beginning of a one millisecond epoch (this means that if the scheduler is disabled in the middle of creating scheduled traffic, all of the ARINC words for that millisecond will get loaded into the various transmit buffers before the scheduler goes idle).

The elements of each Message Table entry are defined as follows:

Element	Element	Description	Host Access Limitations
0	MESSAGE RATE	This element defines the periodic message transmission rate in milliseconds, with the following valid values: 0: entry is disabled/unused 1: transmission every 1 millisecond 0xFFFFFFFF: transmission every 2 ³² milliseconds	None
1	CHANNEL	This element must contain a valid ARINC 429 transmit channel number.	Writable only when entry is disabled.
2	NUMBER OF MESSAGES TO TRANSMIT	This element defines the number of times to transmit this periodic message, with the following valid values: 0x00000000: message disabled, still processed 0x00000001: transmit one word 0xFFFFFFFF: transmit (2 ³²)-1 words 0xFFFFFFFF: unlimited continuous transmission	Writable only when entry is disabled.
3	OFFSET	This element is utilized in two ways. When started, the Message Scheduler assigns this element to the sum of the previous value in this element and the contents of this element to the MESSAGE RATE value. It then decrements the value in this element every millisecond, using it as a counter to track the periodic transmission schedule of this message. Every time this offset value reaches zero, a transmit word is placed in the respective buffer and this value is reset to the MESSAGE RATE value minus one. For the application this element can be used as an initial offset, providing a mechanism to incorporate a delayed transmission of one or more words. This is useful for avoiding message rate skew.	Writable only when entry is disabled.
4, 5, 6	Not Used		
7	DATA	This element defines the periodic message content to be transmitted.	None

Snapshot Buffer

The Snapshot Buffer feature provides the ability to store the latest ARINC 429 message data received on a channel for subsequent recall by the host application. It is implemented as a table of 256 entries/channel, (one entry for each valid ARINC 429 label value), allocated for each of the first sixty-four channels on the board. Each channel/label combination is allotted four 32-bit locations, for a total of 4K words/channel.

Application definition of the Snapshot Storage Mode should be based on the desired use of the Snapshot Buffer feature. Received ARINC 429 messages can be stored in each Snapshot Buffer entry based on the message label value or in one of four separate locations within the entry based on the combined values of the message label and SDI fields. The Snapshot Storage Mode is defined via the SNAPSHOT MODE bit in the Global Enable Register.

A SNAPSHOT MODE bit value of 0 configures snapshot storage based on the message label field value only, while a value of 1 configures snapshot storage based on the combined value of the message label and SDI fields.

Entries in the Snapshot Buffer are accessed using a combination of channel value, ARINC 429 label value, and SDI field value. Combinations of these field values range from channel 0 to 63, octal label value 000 to 377, and SDI field value from 0 to 3. These latter two fields are identified in the ARINC 429 word, with all three used in combination to calculate an offset from the Snapshot Buffer base address as follows:

31 - 16	15 - 10	9 - 2	1 - 0
0	Channel Number (0 - 63)	ARINC 429 Label Bits 7:0 of the ARINC Word	<i>Snapshot Mode = 0:</i> Use SDI Field Value as the offset to message data within this entry <i>Snapshot Mode = 1:</i> Location 1 = 64-bit time-tag lsw Location 2 = 64-bit time-tag msw Location 3 = reserved Location 4 = message data

SRAM Memory Organization

The CEI-x30 device uses several features mapped to the on-board SRAM device, some of which are accessible through the use of the SRAM Address and Data Registers. The memory map and descriptions for the portions of this external memory are defined in the following three paragraphs.

Lword Offset	Read/Write	Device Interface Register Description
0x00000 – 0x0FFFF	Read/Write	Label Filter Table
0x10000 – 0x1FFFF	Read/Write	Snapshot Buffer, (also mapped to Common Memory)
0x20000 – 0x7FFFF	No access	Individual Channel Buffers, allocated as follows:
0x20000 – x2FFFF	No access	Transmit Channel Buffers
0x30000 – x3FFFF	No access	Merged Receive Buffer
0x40000 – x7FFFF	No access	Receive Channel Buffers

Label Filter Table

The Label Filter Table provides a method to program buffer filtering and hardware interrupt generation based on a field-match trigger using a combination of the ARINC 429 message label, SDI, and ESSM field values. This table contains a single 32-bit entry for each combination of ARINC 429 label, SDI, and ESSM values, programmed as eight 4-bit ESSM fields (0 to 7) in individual 32-bit entry locations accessed via combined label (octal 000 to 377) and SDI (0 to 3) values as follows:

Offset 00000 : Label o000 SDI 0
 Offset 00001 : Label o000 SDI 1
 Offset 00002 : Label o000 SDI 2
 Offset 00003 : Label o000 SDI 3
 Offset 00004 : Label o001 SDI 0
 Offset 00005 : Label o001 SDI 1
 Offset 00006 : Label o001 SDI 2
 Etc.

Filtering for each ESSM field value within each 32-bit entry is mapped as follows:

b31-b28	b27-b24	...	b07-b04	b03-b00
ESSM 7	ESSM 6	...	ESSM 1	ESSM 0

The content of each 4-bit ESSM Label Filter Table entry is defined as follows:

3	2	1	0
Unused	Interrupt Enable 0: disabled 1: enabled	Snapshot Filter Enable 0 : unfiltered 1 : filtered	FIFO Filter Enable 0 : unfiltered 1 : filtered

When the Snapshot or FIFO Filter enable bit is zero for a specified label/SDI/ESSM combination, any message received containing that combined field value is recorded in the respective buffer. When the respective filter enable bit is set to one for a specified label/SDI/ESSM combination, any message received containing that combined fields value is not recorded in the respective buffer. The FIFO Filter Enable bit

enables/disables filtering to either the regular or merged receive buffer, depending on how this channel is programmed.

When the respective Interrupt Enable bit is set to one for a specified label/SDI/ESSM combination, any message received containing that combined field value will trigger an entry in the Interrupt Queue. If the INTERRUPT ENABLE bit is set to Enabled in the Global Enable Register, a PCI interrupt is also generated.

Snapshot Buffer

The Snapshot Buffer is mapped to the Device Interface Register Set, located in common memory, described in a previous section of this document.

Individual Channel Buffers

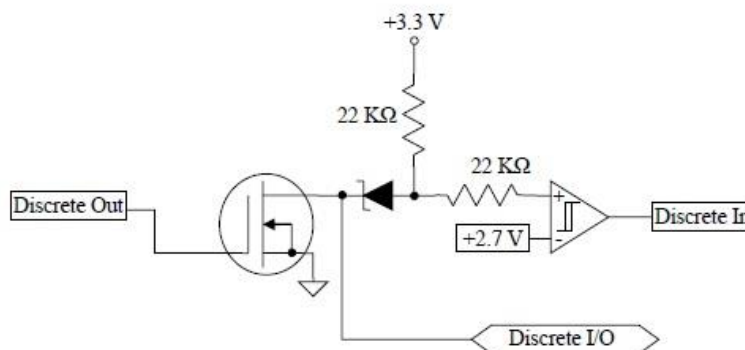
The Individual Channel Buffers provide storage for all transmit and receive FIFO buffers. All host interaction surrounding the use of the FIFO buffers is described in the respective Channel Buffer Word paragraphs, with the underlying memory inaccessible to the host interface.

ARINC 429 Receive Threshold

The ARINC 429 Receive Threshold is configured at the factory to be nominally +/- 3.0 volts, and is not user selectable.

Avionics Discrete I/O

Most CEI-x30 cards provide up to sixteen bi-directional individually configurable Avionics Discrete channels, while the RAR-XMC, RAR-EC, RCEI-830A, and CEI-830 optionally provide up to four independent Avionics Discrete input/output channels. Avionics Discrete I/O is used for general avionics-level I/O interfacing. The discrete outputs are low side n-channel FET switches capable of sinking 500mA, while the inputs are single ended, protected (50V max), with a logic threshold of approximately 2.7V. The basic circuit for a bi-directional discrete I/O channel is shown below:



Discrete Outputs

The discrete output channels have the following truth-table functionality:

Discrete Out	Discrete I/O pin
1	FET ON [conduct to Ground]
0	FET OFF [tri-state]

To assign Discrete Output states using the AR_SET_DEVICE_CONFIG API call with the item parameter value ARU_DISCRETE_OUT, valid value parameter selections are:

AR_LO	Discrete Output set to 1 (FET ON – conduct to Ground)
AR_HI	Discrete Output set to 0 (FET OFF – tri-state)

Discrete Inputs

When bi-directional discrete pins are disconnected from any external signal, Discrete In reflects the value of Discrete Out. When the FET is on, reading Discrete In should return a “0”. When the FET is off, reading Discrete In generally returns a “1” (because of the weak 22 KΩ pull-up resistor) but the load attached to the discrete I/O pin must also be taken into consideration.

The discrete input channels have the following truth-table functionality:

Discrete I/O pin	Discrete In
> 2.7 VDC	1
< 2.7 VDC	0

When a Discrete Input is connected to an external circuit, reading the state via AR_GET_DEVICE_CONFIG invocation with the item parameter ARU_DISCRETE_IN will result in one of the following return values:

AR_HI	Discrete Input is 1
AR_LO	Discrete Input is 0

Differential Discrete I/O

The CEI-430 provides up to four individually configurable RS-485-level differential input/output channels. RS-485 differential channels are suitable for discrete signaling requiring long cable runs or when requiring true differential signaling.

The Differential I/O channel receive data always reflects the state of the channel's I/O pair. The receive truth table is listed below.

Differential I/O	Differential Input Data
DIFF+ \geq DIFF- by 300mV	1
DIFF+ \leq DIFF- by 300mV	0
DIFF+ and DIFF- shorted	1
DIFF+ and DIFF- floating	1

The Differential Discrete transmitter section requires the Differential Transmit Enable bit to be set in order for the transmitter to function.

Differential Enable	Differential Transmit	Differential I/O
0	X	Hi-Z
1	1	DIFF+ > DIFF-
1	0	DIFF+ < DIFF-

Hardware Channel Assignments

While the hardware channel assignments may change with firmware revisions, the API handles the actual channel indexing internally. The following channel index values are used by the API internally:

Channel Index Value	Channel Assignment
0 through 31	ARINC 429 Receive Channels
32	ARINC 717 Receive Channel
63	Merged Mode Receive Buffer
64 through 95	ARINC 429 Transmit Channels
96	ARINC 717 Transmit Channel
128 through 191	Discrete Input Channels
192 through 207	Discrete Output Channels